Université catholique
de Louvain

Laboratoire de Microélectronique
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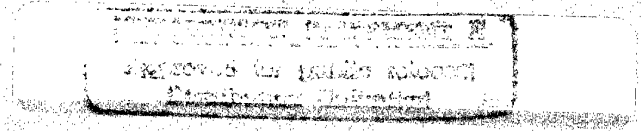
Double-gate SOI/MOS devices and circuits in hostile environments



Pascale Francis

Thèse présentée en vue de l'obtention
du grade de Docteur en Sciences
Appliquées

Promoteur: **Pr. J.P. Colinge**

Jury: **Pr. S. Cristoloveanu**
Dr. G.E. Davis
Dr. J. Ladrière
Pr. F. Van de Wiele

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Ami, ne sois pas perfectionniste,
Le perfectionnisme est un fléau, une tension
Qui te fait trembler de peur de rater ta cible.
Laisse-toi du champ et tu seras parfait.

Frédérick S. Perls.

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Contents

Notations

Most notations used throughout the text are gathered here for convenience.

β_{eff}		effective bipolar amplification gain
β_n	$= \mu_n(W/L)_n C_{ox}$	electron current scaling factor
β_p	$= \mu_p(W/L)_p C_{ox}$	hole current scaling factor
c_{Si}		specific heat of silicon
c_{SiO_2}		specific heat of silicon dioxide
C_{ox}	$= \varepsilon_{ox}/t_{ox}$	gate oxide capacitance
C_{si}	$= \varepsilon_{si}/t_{si}$	film capacitance
C_L		loading capacitance
C_T		equivalent capacitance of an SRAM cell
D		dose (ex: rad(Si))
$\dot{D}$		dose rate (ex: rad(Si)/s)
D_{it}		interface state density
D_n		electron diffusivity
ΔT		channel temperature elevation
ΔT_g		gate temperature elevation
ΔV_{it}		threshold voltage shift due to interface traps
ΔV_{ot}		threshold voltage shift due to oxide charges
$E(x)$		electric field
E_{e^-/p^+}		energy required to produce an el./hole pair
E_g		silicon bandgap
E_{sat}		lateral electric field at the edge of the velocity saturation region
E_S	$= E(-t_{si}/2)$	surface electric field
ε_{ox}		permittivity of silicon dioxide
ε_{si}		permittivity of silicon
$\phi(x)$		channel potential
ϕ_{ms}	$= \pm(E_g/2) - (kT/q)\ln(N_A/n_i)$	work function difference between the N^+ or P^+ polysilicon gate and the P^- film.
ϕ_F	$= (kT/q)\ln(N_A/n_i)$	Fermi potential
ϕ_0	$= \phi(0)$	mid-film potential
ϕ_S	$= \phi(-t_{si}/2)$	surface potential
g_m	$= \partial I_D/\partial V_{GS}$	transconductance
g_D	$= \partial I_D/\partial V_{DS}$	output conductance
G_{ch}		channel thermal conductance/unit area
G_g		gate thermal conductance/unit area

$G_{s,d}$	- S/D thermal conductance/unit area
G_T	- global thermal conductance
G_{Tch}	- channel thermal conductance
G_{Tg}	- gate thermal conductance
$G_{Ts,d}$	- S/D thermal conductance
I_{bias}	- bias current
I_{crit}	- critical current to cell upset
I_{leak}	- leakage current
I_{sat}	- saturation current
I_D	- drain current
I_G	- gate current
J_{ch}	- heat flow through the channel region
J_g	- heat flow through the gate region
$J_{s,d}$	- heat flow through S/D regions
J_{ns}	- instantaneous electron current density at the source edge
J_{ps}	- instantaneous hole current density at the source edge
k	- Boltzmann constant
κ_{SiO_2}	- thermal conductance of silicon dioxide
κ_{SiN^+}	- thermal conductance of N^+ (poly)silicon
L	- device drawing length
Ld	- length of the drain region
L_{eff}	- device effective length
L_g	- effective gate length
L_{ov}	- overlap of the back-gate below S/D regions
Ls	- length of the source region
L'	- drawing length of the cavity
L''	- effective length of the cavity
LET_{eff}	- effective Linear Energy Transfer
LET_0	- normally incident Linear Energy Transfer
λ	- natural scaling length
Λ_g	- gate temperature decay length
$\Lambda_{s,d}$	- S/D temperature decay length
μ_{bulk}	- volume mobility
μ_n	- electron mobility
μ_p	- hole mobility
n	- body effect factor
n(x)	- electron concentration
n_i	- intrinsic carrier concentration
N_A	- channel doping concentration
$n_0 = n(0)$	- mid-film electron concentration
$n_S = n(-t_{si}/2)$	- surface electron concentration
υ_{sat}	- saturation velocity
P	- total dissipated power
q	- electronic charge

Q_{col}		- collected charge after a heavy ion hit
Q_{crit}		- critical charge to cell upset
Q_{inj}		- charge injected by a heavy ion hit
Q_{ox}	$= qN_{ox}$	- density of oxide charges
Q_D	$= qN_A t_{si}$	- total depletion charge
Q_N		- total charge of free carriers
θ	$= \theta' + R_{sd}(\mu C_{ox} W/L)$	- mobility attenuation factor
θ		- impinging angle
θ'		- intrinsic mobility attenuation factor
R_c		- characteristic radius of a plasma track
R_{ext}		- external resistance
R_g		- channel thermal resistance/unit area (lateral)
$R_{s,d}$		- S/D thermal resistance/unit area (lateral)
R_{sd}	$= R_S$	- S/D series resistance
R_T		- equivalent resistance of an SRAM cell
ρ_{Si}		- density of silicon
ρ_{SiO_2}		- density of silicon dioxide
S_n		- (inverse) subthreshold slope in nMOSFETs
S_p		- (inverse) subthreshold slope in pMOSFETs
$t_{backgate}$		- back-gate thickness
t_{ox}	$= t_{oxf}$	- (front) gate oxide thickness
t_{oxb}		- buried oxide thickness
t_{oxe}		- edge oxide thickness
t_{si}		- silicon film thickness
t_{top}		- thickness of the top passivation layer
T		- absolute temperature
τ		- heating time constant
τ_g		- generation lifetime in depletion regions
τ_r		- recombination lifetime in neutral regions
τ_A		- access time of an SRAM
τ_F		- fall time of an output swing
τ_R		- rise time of an output swing
V_{dd}		- supply voltage
V_{in}		- input voltage
V_{out}		- output voltage
V_{BD}		- breakdown voltage
V_{BS}	$= V_B - V_S$	- substrate-to-source voltage in SOI
V_{DS}	$= V_D - V_S$	- drain-to-source voltage
V_{Dsat}		- voltage drop across the non-saturation channel region
V'_D		- corrected drain voltage
V_{EA}		- Early voltage
V_{FB}		- flat-band voltage
V_{GS}	$= V_G - V_S$	- gate-to-source voltage
V'_G		- corrected gate voltage
V_S	$= 0$	- source voltage

V_{Si}	-	volume of silicon
V_{SiO_2}	-	volume of silicon dioxide
V_{th}	-	threshold voltage
V_{ZTC}	-	Zero Temperature Change gate voltage
W	-	device drawing width
W_{eff}	-	device effective width
W'	-	drawing width of the cavity
W"	-	effective width of the cavity
x_{dmax}	-	maximum depletion region
$X[\theta]$	-	geometrical reduction factor of Q_{inj}

Introduction

Bulk silicon Complementary-Metal-Oxide-Semiconductor (CMOS) is the dominant market technology in the digital integrated circuit world with two main drivers: memory devices and microprocessors. In the bulk MOS technology, the interaction between the active devices and the semi-infinite substrate results in parasitic effects such as the latchup (the unwanted triggering of parasitic pnpn thyristors formed by CMOS bulk structures in their well) and large parasitic capacitances (inherent to the reverse-biased junctions that isolate the devices from one another). When technology dimensions shrink, latchup becomes a severe problem because the gain of the parasitic bipolar structures becomes large. Also, higher substrate doping concentrations are used, which increases junction capacitances. A solution to these problems is found by isolating the device from the substrate.

Since the beginning of the eighties, several techniques have been developed for producing a thin film of single-crystal silicon on top of an insulator [1]. In these Silicon-on-Insulator (SOI) technologies, devices are dielectrically isolated from the others. Switching from junction to dielectric isolation suppresses wells and offers tremendous advantages: the latchup and leakage paths between devices are ruled out, the fabrication process is simplified and the integration density is increased. Also, the presence of the insulator layer (generally SiO_2) suppresses the well-to-substrate and fringing field capacitances. In addition, the polysilicon- and metal-to-substrate capacitances are limited by the buried insulator capacitance, which is typically lower than the junction capacitance of a bulk MOSFET. For the same reason, the drain/source-to-substrate parasitic capacitances are reduced by a factor 4 to 7 and are much less sensitive to the supply voltage. Finally, the buried insulator thickness does not necessarily have to be scaled down as device dimensions are reduced which reinforces the capacitance reduction advantage of SOI over bulk in submicron technologies. Keeping parasitic capacitances as low as possible is crucial to decrease dynamic consumption and improve speed performance.

SOI MOSFETs are highly dependent on the thickness of the silicon film in which they are made and on the channel doping concentration. Different types of SOI transistors can be distinguished: "partially depleted" (PD) devices in thicker films (over 200nm) and "fully depleted" (FD) enhancement mode (EM) or accumulation mode transistors (AM) in thinner films.

In "partially depleted" devices, the silicon film is never fully depleted underneath the gate electrode. There is no coupling between the front gate and the back gate. The device

basically operates as a bulk transistor with the advantages of dielectric isolation and parasitic capacitances reduction. Nevertheless, new parasitic "floating body" effects arise from the non-depleted (neutral) portion of the active silicon region [2]. There are essentially three of them: the kink effect, which degrades the output impedance of the devices, the reduction of the drain breakdown voltage, and the subthreshold hysteresis/latch phenomenon. All of these effects have the same basic origin. In an SOI nMOSFET, holes created by impact ionization at the drain form a hole current which travels through the body, raising the body potential which, in turn, increases the electron MOS current to the drain. One possible solution is to fix the body potential by adding a fifth terminal to the device, the so-called body tie. This solution is nevertheless prohibitively area consuming.

Another way to solve the kink problem is to suppress the neutral region by thinning the silicon film [3,4]. "Fully depleted" (FD) devices are then obtained where the silicon is fully depleted underneath the gate electrode so that the charge-control of the gate on the channel is increased. An image of the resistance opposed by the device to let the gate electrode modify its surface potential, and hence its current, is the body-effect coefficient n which is significantly lower in FD SOI devices than in bulk transistors. Typically, n is 1.15...1.5 in bulk and 1.05 in FD SOI. The lower the coefficient, the more ideally the device behaves. One can indeed easily demonstrate that the reduction of the body-effect factor implies near-ideal subthreshold swing [5,6,7] and lower transverse electric field, which in turn results in a higher effective channel mobility [8] and a higher drain saturation current [9]. On the other hand, the smaller charge sharing between drain and channel regions reduces the short-channel threshold voltage roll-off [10].

In "accumulation-mode" (AM) devices, the channel is composed of majority carriers. AM devices exhibit a high mobility, no kink, and very little bipolar effects but are more sensitive to punchthrough than regular "enhancement-mode" (EM) devices [11].

The choice between FD and PD options is still recognized as the main SOI front-end technology tradeoff [12]. FD devices pose several technological problems related to their very thin film such as large source/drain series resitances while PD devices could pose circuit design problems due to their prominent floating-body effect. The choice is even less obvious since dynamic floating-body effects have been observed in scaled FD devices [13].

The advantages of using the SOI technology and, more particularly, FD or AM SOI devices, are so numerous that SOI CMOS has the potential of becoming the mainstream technology for future high performance applications.

- The steepest subthreshold slope allows to lower the threshold voltage, and hence to reduce the supply voltage, for same speed performance while preserving the same leakage current level. This leads to low power and/or low voltage high-speed operation of digital as well as analog circuits [14,15,16,17,18,19,20]. Recent examples are demonstrations of a 64bit adder with a critical delay of 1.9ns at 3.3V [21] and a 5.7Mhz 0.9V microcontroller CPU [22]. The full dielectric isolation also provides

advantages in terms of linearity by suppressing the non-linear drain-to-bulk junction capacitances encountered in standard technologies [23]. It also allows the integration of mixed-signal components on the same chip by minimizing clocking feedthrough.

• SOI is very promising in the microwave frequency domain as well. Conventional bulk-Si technologies cannot be used because the high-resistivity silicon substrate, required in the Ghz range [24,25,26], cannot be obtained. Indeed, even small quantities of dopant diffused during the process degrade the resistivity substantially. On the contrary, the insulating layer of SOI wafers efficiently preserves the high purity of the substrate during circuit fabrication so that SOI MOSFETs offer excellent microwave performance competitive with GaAs circuits: small losses, crosstalk and substrate-coupling effects as well as high gain cut-off frequencies in the range 10-25Ghz have been demonstrated [27,28,29,30,31]. First reports on optical waveguide switches [32,33] prove that SOI has also a large potential for low cost optical devices.

• SOI can be used for quantum device fabrication [34,35,36,37,38].

• SOI CMOS circuits can be operated at substantially higher temperature than bulk circuits [39,40,41]. Their threshold voltage dependence on temperature is significantly reduced owing to the higher charge-control of the gate on the channel region. Furthermore, the leakage current of SOI MOSFETs is several orders of magnitude smaller at high temperature than that of bulk devices because the leakage of the well junction is suppressed. In addition, the leakage of the reverse-biased drain junction is efficiently limited owing to the reduction of the drain junction area.

• Finally, the radiation effect community has long recognized the benefits of the SOI technology. SOI devices are inherently harder than bulk devices to transient effects such as Single-Event-Effects (SEE) and gamma-dot effects because the buried oxide layer prevents the charges generated within the substrate to be collected by the device junctions [42,43,44,45]. However, if the back-gate bias is such that the substrate under the buried oxide is depleted, SOI devices are not totally insensitive to back funneling in the substrate [46]. This effect is not observed with the substrate underneath the buried oxide in inversion or accumulation. Also, the parasitic lateral bipolar amplification of the current spike created by the particle impact can reduce the benefit of the dielectric isolation in floating body devices.

Despite its obvious advantages, the SOI technology still presents some difficulties precisely arising from the presence of the thick buried insulator layer.

• Permanent effects of radiative environments are worse in SOI than in bulk [47] because charge trapping, inducing parameter shifts, increases with the thickness of the oxide layers in contact with the active channel. Therefore, high total-dose hardness does not come for free and can only be achieved by shielding the channel from the thick buried oxide layer [48]. This modification of the fabrication process unfortunately implies the use of PD devices.

• The heat evacuation towards the substrate is drastically reduced in SOI devices since the buried oxide layer has a poor thermal conductivity. As a results, annoying self-heating phenomena linked to high power operation are enhanced [49,50,51].

To minimize the above mentioned problems, one could think of scaling the buried oxide [52]. Such a scaling would also efficiently delay punchthrough and short channel effects [53] and reduce the fabrication cost of SIMOX wafers. On the other hand, the subthreshold swing would get worse due to stronger backside coupling [1] and the SEU sensitivity related to back funneling in substrate would be enhanced. Also, speed performance would degrade as a results of larger parasitic capacitances with substrate and current drive reduction [52]. Finally, in case of DRAMs, the increase of the bit line capacitance would not only affect speed by slowing bit-line sensing but would also increase the lower limit of the memory cell capacitance, especially at low voltage operation [54].

Another very elegant solution consists in realizing symmetrical structures with an insulated gate at the bottom part of the channel, electrically tied to the front gate. Assuming that the back gate oxide is as thin as the front gate oxide, these new devices consist of two identical MOS transistors working in parallel, one at the front and one at the back interface of the active silicon region. Recently, such FD double-gate symmetrical devices have been fabricated starting from SIMOX wafers [55]. They consist of a thin channel region totally wrapped in a thin high-quality gate oxide, which is itself totally surrounded by a polysilicon gate. For this reason, they are called surrounding gate or Gate-All-Around (GAA) devices. The major drawbacks of the SOI technology related to the presence of the buried oxide below the channel (poor total-dose hardness, self-heating effects) should be solved, since the channel is totally surrounded by a thin oxide layer only. Parasitic capacitances are only slightly increased because source and drain still lie on a thick buried oxide. Furthermore, some electrical characteristics of regular FD SOI devices, such as short channel effects, transconductance and subthreshold slope, should be further improved as a result of the nearly perfect coupling between the gate and the channel potential, that arises now symmetrically from both sides of the film. The body factor is equal to unity and the device is inherently free of substrate coupling. The GAA SOI device is hence expected to be the ultimate (or ideal) MOSFET.

This dissertation presents the research related to this GAA device. In Chapter I, the fabrication process is described, and electrical characteristics are presented. The particular physics of volume inversion-mode devices, resulting from the stronger gate control on the channel potential, is analyzed in detail in Chapter II. One-dimensional models of the potential distribution are discussed from which accurate expressions of the drain current, the transconductance, the threshold voltage and the subthreshold current are derived.

The following chapters deal with different kinds of hostile environments where GAA devices outperform regular SOI transistors. Chapter III demonstrates that GAA transistors benefit from minimum threshold voltage roll-off up to a higher temperature than SOI (and of course bulk) devices. Chapter IV proves that self-heating effects, appearing at large power operation, are reduced in the GAA structure compared to the

regular SOI technology, owing to the thinning of the oxide layers which separate the channel region from the substrate.

The last three chapters, V through VII, focus on the tremendous benefits provided by the GAA transistor for applications requiring a high level of radiation-hardening such as space, military or nuclear industry applications. The new structure is shown to adequately solve both permanent and transient radiation-related problems. Chapter V presents the inherently large cumulated-dose hardness of the GAA device which arises from both the process and the geometry. Chapter VI deals with new circuit designs to improve the total-dose hardness of simple logic blocks and static random access memories. It is shown that circuit skills could never mitigate irradiation-induced leakage currents at a reasonable expense of chip area. The only solution consists in using a hardened technology such as the GAA process. Finally, a new dynamic analysis is developed in Chapter VII to explain the measured insensitivity of GAA static memories to current spikes created by heavy particle hits.

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Chapter I:
The Gate-All-Around device

It can be shown that the optimum MOSFET is a device where the substrate would have rigorously no influence on the electrical characteristics. With the object of minimizing the substrate effect, several techniques have been developed during the eighties for producing a thin-film of single-crystal silicon on top of an insulator (SOI) [1]: zone-melting recristallization (ZMR) [2], epitaxial lateral overgrowth (ELO) [3], full isolation by porous silicon (FIPOS) [4], separation by oxygen implantation (SIMOX) [5], and bonding and etch-back SOI technique (BESOI) [6]. SIMOX and BESOI have now emerged as most attractive. SIMOX is chosen for fabricating thin-film SOI wafers where good film thickness uniformity is required (e.g. for CMOS applications), and BESOI is usually used for the production of thick-film SOI layers where a very low defect density and a thick buried insulator layer are required (e.g. for high-voltage device applications). The principle of SIMOX material formation is very simple and consists in the creation of the SiO_2 buried layer by implantation of oxygen followed by an annealing step. To obtain a BESOI wafer, two oxidized wafers are "bonded" together by simple contact. The strength of the bond is subsequently improved by annealing. One of the wafers is then polished or etched down to a thickness suitable for SOI applications. The other wafer serves as a mechanical substrate, and is called handle wafer. Very recently, a new technique based on wafer bonding provides a silicon-on-insulator material which has both a very high thickness uniformity and a very low defect density, while only requiring a single bulk wafer [7]. It involves a heat treatment which induces an in-depth micro slicing of one of the two bonded wafers previously implanted with hydrogen.

The optimum electrical properties that could be achieved by fully-depleted SOI devices are more closely approached with either the use of an infinitely thick buried insulator or by adding an insulated gate at the bottom part of the channel to shield the substrate effect. In the latter solution, further requirements are having same front and back gate oxide thicknesses and tying front and back gates electrically together. This theoretical concept of symmetrical double-gate devices dates back to 1984 [8]. The device is then called XMOS which originates from the resemblance of the symmetrical structure with the Greek letter Ξ.

Four more years were necessary for the first practical realizations to arise which involved, at first, complicated, highly non-planar processes. The Surrounding Gate Transistor (SGT) proposed by Takano *et al.* in 1988 is made of a silicon pillar surrounded by the gate electrode [9,10]. Source, gate and drain are arranged vertically, the

sidewalls of the silicon pillar being the channel (Figure 1.1A). Such devices have dramatically increase the integration density of ULSI circuits and DRAMs [11,12,13,14]. A different implementation of the same concept, the gate control of vertical ultra-thin SOI structures, is proposed in 1989 by Hisamoto *et al.* [15,16]. Their device is called Fully DEpleted Lean-channel TrAnsistor (DELTA). It is made of vertical silicon islands etched on the top of the substrate and capped with nitride spacers. The substrate is then oxidized which leads to the formation of SOI structures owing to the growth of some oxide underneath the protected silicon walls (bird's-beak-like effect). The nitride spacers are then removed and the rest of the fabrication is similar to conventional self-aligned processes. In this structure, source, gate and drain are hence arranged horizontally (Figure 1.1B).

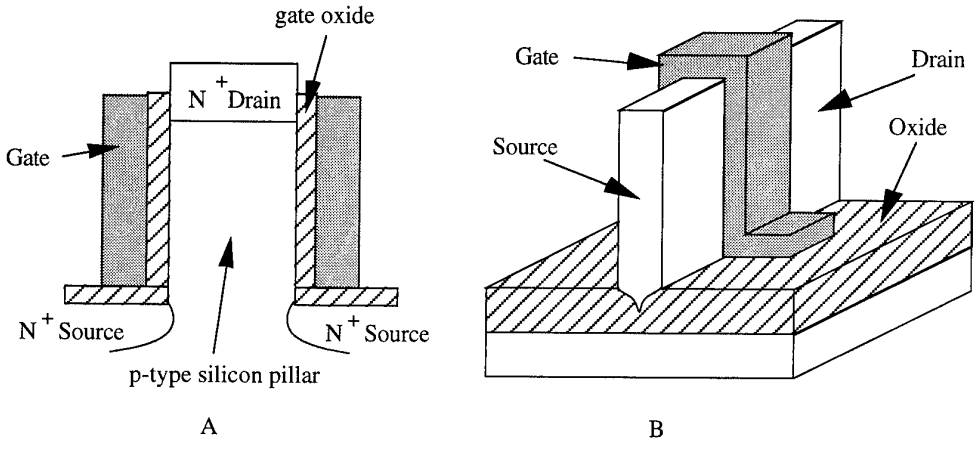

Figure 1.1: A) Vertical Surrounded Gate Transistor (SGT) [9,10] and
B) Fully DEpleted Lean-channel TrAnsistor (DELTA) [15,16].

More attractive planar structures have recently emerged, proposing the double-gate control of horizontal SOI films. These structures have been obtained either by solid-phase epitaxy (SPE) of a Si film deposited by chemical vapor deposition (CVD) of SiH_4 over a lower-gate oxide (Figure 1.2A) [17], or by ELO of the Si film over an oxidized buried gate, followed by a chemical-mechanical polishing (CMP) step (Figure 1.2B) [18,19]. A second gate is then fabricated on top of the device.

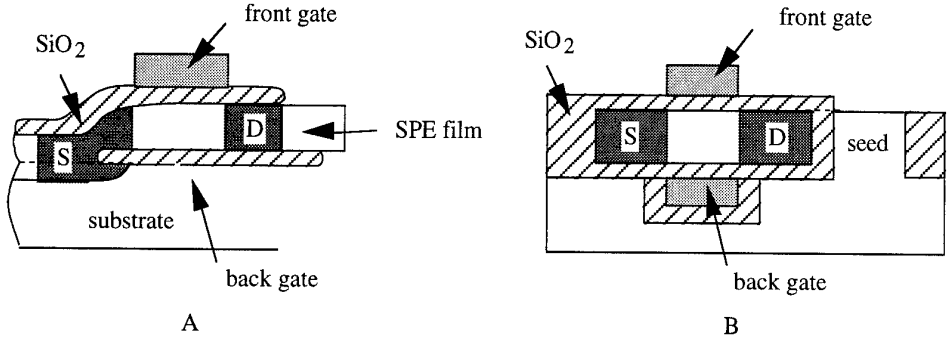

Figure 1.2: Planar double-gate structures:
A) SPE of SiH_4 CVD of over a lower-gate oxide [17] and
B) ELO of the Si film over an oxidized buried gate [19].

Another technique takes advantage of the wafer bonding process [20,21]: bottom gates are formed on a first wafer and covered by a thick layer of CVD SiO_2 planarized by polishing. This oxide is then bounded on a base wafer so that the initial substrate of the first wafer can be thinned down to become the active Si channel. SOI MOSFETs are finally realized on top of the bottom gates by conventional methods. From the above mentioned techniques, wafer bonding is probably one of the most promising candidate owing to full compatibility with conventional ULSI designs. However, it requires several selective polishing steps and does not ensure alignment of front and back gates.

This chapter will deal with our own experience of double-gate devices [22], called Gate-All-Around (GAA) MOSFETs because the silicon in the channel area is completely wrapped in the gate oxide and the gate electrode material. Although not fully optimized, this process provides, to our knowledge, the only symmetrical, self-aligned, and planar double-gate structure realized starting from SIMOX wafers. Furthermore, the Gate-All-Around process is similar to the process sequence used to produce regular SOI devices with only one additional masking step and one wet etch step of the buried oxide.

A variation of our technique has been used to produce thin-film poly-Si channels totally surrounded by a polysilicon gate [23]. A dummy nitride pattern is first formed across which the poly-Si channel is deposited. The nitride pattern is then removed leaving the channel floating in the air like a bridge. Next, gate oxide is grown and gate poly-Si is deposited all around the channel.

Though they bear similar names, the double-gate or dual-gate concept should not be mistaken with the twin-gate concept [24] (cascade of master and slave transistors used to improve the breakdown voltage and the output impedance) nor with the dual-poly gate concept [25,26] (technology where both N^+ and P^+ doped gates are available so that both nMOS and pMOS could be surface channels).

After the description of the GAA device fabrication, specific layout rules will be quickly examined, scaling will be discussed and electrical characterization will be presented, pointing out the numerous advantages of the new structure.

1. GAA device fabrication

The process starts with standard <100> SIMOX wafers with a substrate resistivity of 20Ωcm (corresponding to $N_A = 7\times10^{14}cm^{-3}$). The initial thickness of the silicon film is 180nm. This top silicon layer is first thinned down using dry oxidation and oxide strip in buffered HF in order to obtain a silicon film thickness of 85nm at the end of the process. A 25nm-thick pad oxide is then grown, and a 200nm-thick silicon nitride film is deposited. The nitride and the pad oxide are patterned in a dry etch reactor and will protect the future active silicon areas. Masking p-channel devices, a rather heavy dose of boron is then implanted to increase the threshold voltage of the lateral n-channel transistors such as to avoid edge transistor turn-on (Figure 1.3A). Using the nitride pattern as a mask, the silicon film is now patterned by plasma etching to define the insulated active areas (mesa process). Before removing the nitride layer, a wet oxidation

at 900°C is performed which aims at smoothing the edges (or corners) of the silicon islands (Figure 1.3B). This has been reported to usefully improve the gate oxide breakdown properties [27]. The duration of this oxidation cannot be too long, otherwise a detrimental triangular shape of the edges is obtained as well as the segregation of most of the implanted boron. The optimum oxidation time was found to be 20 minutes. The nitride and the pad oxide are finally stripped.

The masking step specific to the GAA process is then used to cover the entire wafer with resist except areas where the buried oxide (as well as the oxide formed at the edges of the silicon islands) will be removed. These areas correspond to an oversize of the intersection between the active island and the future polysilicon gate layer. The wafers are immersed in buffered HF and the subsequent etching of the buried oxide leaves a beam (bridge) of silicon, free-standing over a cavity (Figures 1.3C and 1.4). The silicon bridge is now only supported by the original buried oxide at its ends so that both its width and length must be kept small in order to avoid mechanical fracture.

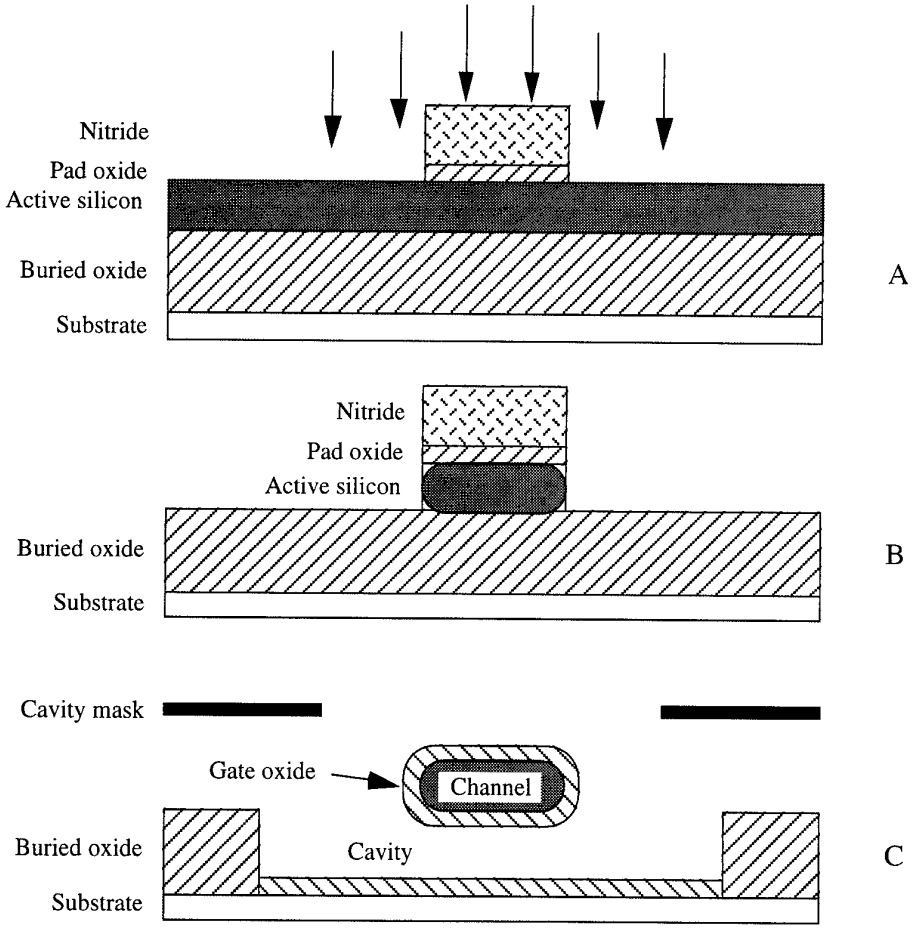

Figure 1.3: Successive steps of the Gate-All-Around device fabrication.

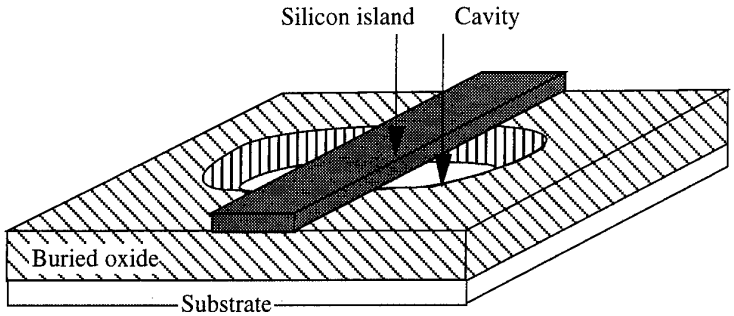

Figure 1.4: Gate-All-Around device after etching of a cavity underneath the silicon island.

The 30nm-thick thermal gate oxide is then grown at 950°C in dry oxygen. The gate oxide grows over all the exposed silicon (top, bottom and edges of the active areas, as well as on the silicon substrate in the bottom of the cavity) (Figure 1.3C). Boron is then implanted to adjust successively the n- and p-channel threshold voltages. A 340nm-thick polysilicon film is deposited in a LPCVD furnace at a temperature of 625°C.

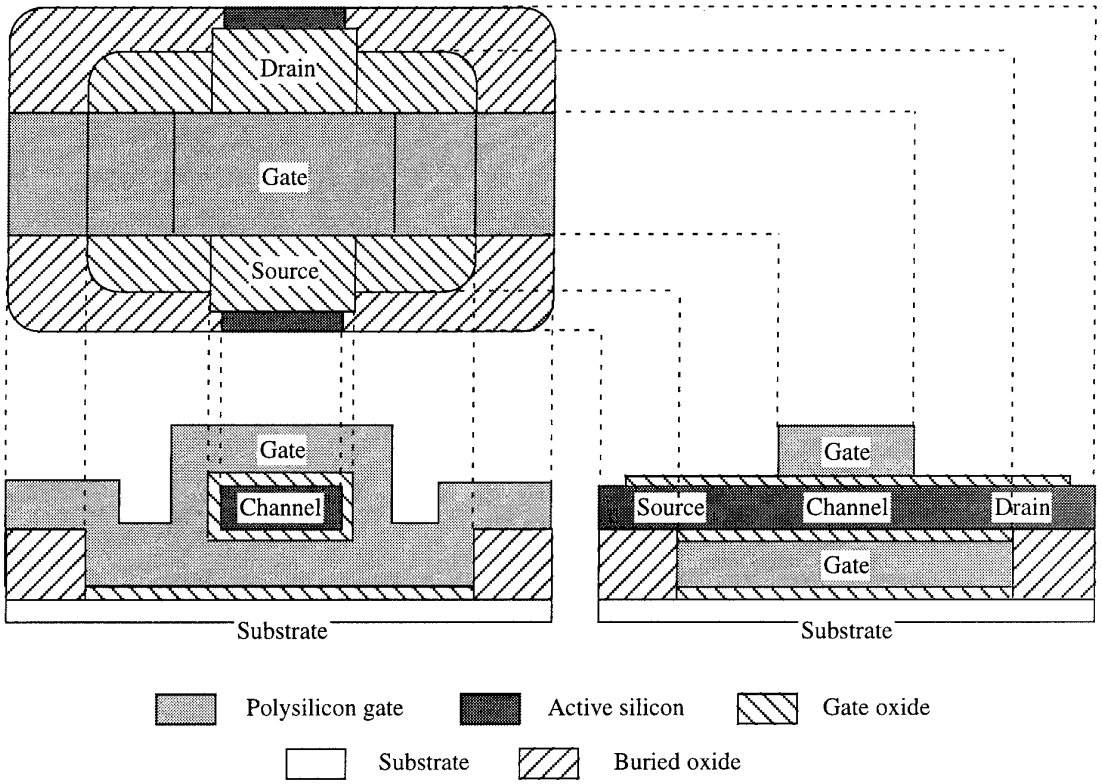

Figure 1.5: Gate-All-Around device after source and drain formation:
top view, lateral and longitudinal cross-sections.

Owing to the excellent step coverage of LPCVD polysilicon, the gate material not only surrounds the top of the device, but also fills the cavity below the silicon bridge (Figure 1.5). Consequently, polysilicon wraps all around the gate oxide which is grown all around the channel region (hence the name: Gate-All-Around device). The polysilicon film is doped with solid source phosphorus in a furnace at 825°C during two hours. The phosphorous drive in (performed together with the source and drain annealing) ensures

that the dopant diffuses everywhere in the polysilicon layer, even underneath the silicon bridge. The polysilicon gate is then patterned using conventional lithography and chlorine-based RIE plasma etching. The good anisotropy of the process leaves polysilicon on the edges of the devices such that some isotropic etching is then used to avoid any leakage. Source and drain are formed using phosphorous (nMOS) or boron (pMOS) implantation (at 20keV) followed by an annealing step during 3 hours and 20 minutes at 850°C.

A low temperature 500nm-thick oxide layer is deposited, contact holes are wet etched and a standard S-gun metallization with an aluminum/silicon alloy is carried out. After half an hour post-metallization sintering at 420°C, the deposition of a 500nm-thick protecting oxide layer on top of the device finally completes the process. Figure 1.6 presents a SEM micrograph of the transversal cross-section of the resulting final GAA device.

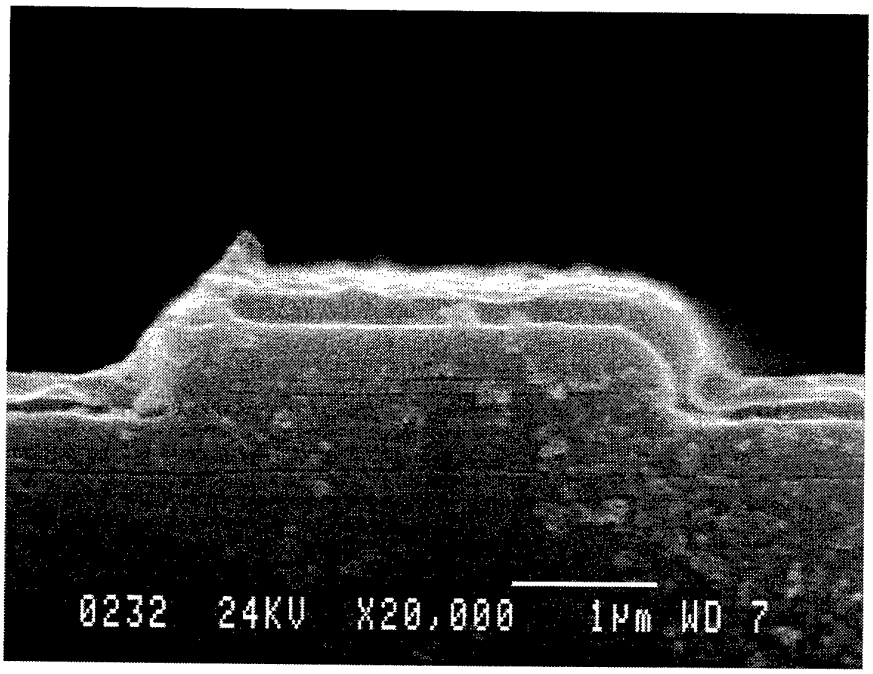

Figure 1.6: SEM micrograph of the final GAA device: transversal cross-section.

2. Specific layout rules

The standard process available in our laboratory ensures a correct reproducibility of structures with drawing sizes greater than 3µm. A minimum size device, with both length L and width W equal to 3µm, is depicted in Figure 1.7. The additional mask specific to the GAA structure, that is necessary to open areas where the underlying buried oxide is removed (called cavities), is also shown. Let L' and W' be the length and width respectively of the drawn cavity. W' is obtained from the minimum device width W when adding x = 1.5µm along the gate in both directions. This extension compensates for the possible ±1µm misalignment of the lithography stepper. Owing to this precaution, the buried oxide HF etching occurs from both sides of the silicon bar, even in the worst case of misalignment. The etching duration can therefore be calculated to remove the buried oxide only on a depth equal to W/2 while still ensuring that the cavity is entirely opened below the silicon bridge. Since the wet etching is isotropic, the final dimensions of the cavity L" × W" are obtained from the drawing mask extended by W/2 in all directions which yields:

$$L'' = L'+W \text{ and } W'' = W'+W = 2(W+x) \qquad (1\text{-}1)$$

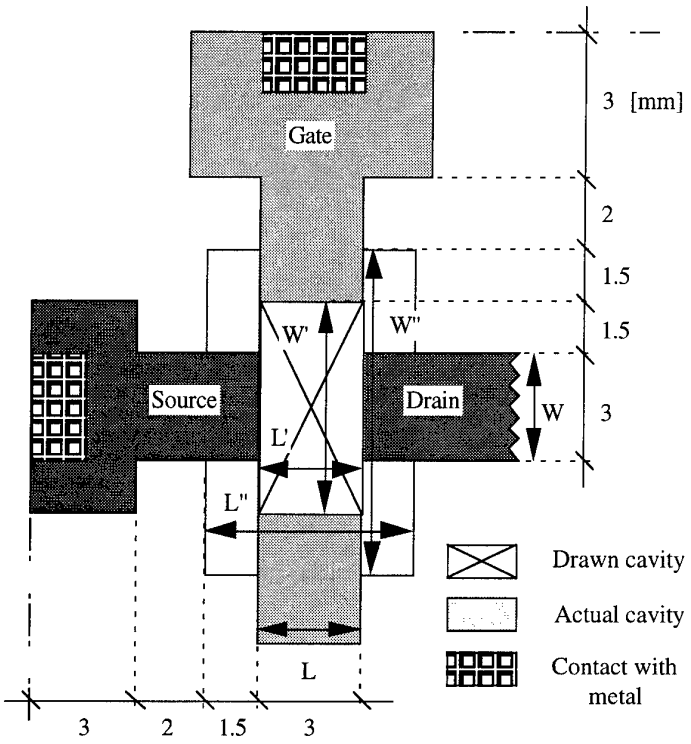

Figure 1.7: Minimum size square GAA device.

If L" exceeds the desired device length L, the cavity extends below the source and drain regions. The polysilicon gate that fills the cavity below the silicon bridge is protected during gate patterning and cannot be removed. Therefore, if the gate mask is perfectly aligned with respect to the cavity, the back portion of the gate finally extends below both source and drain regions over:

$$L_{ov} = (L''-L)/2 = (L'+W-L)/2 \quad (1\text{-}2)$$

as shown in the longitudinal cross-section of Figure 1.5. These overlaps are detrimental to the device performance because they generate increased gate-to-source/drain parasitic capacitances. Furthermore, metal strips are not allowed to run in a 2µm-wide ring around the actual cavity (Figure 1.7) in order to avoid problems linked to the less planar topology in the cavity region (Figure 1.5). The source/drain contacts are subsequently situated 3.5µm+L_{ov} away from the gate edge. As a consequence, source/drain series resistances, which are unfortunately not negligible in very thin silicon films (smaller than 100nm), are increased. If the front gate is misaligned with respect to the cavity, a strong asymmetry between source and drain parasitics appears.

In order to minimize the extension of the cavity below the source and drain regions, and hence to improve compactness and speed, relationship (1-2) shows that L', the drawing length of the cavity, should be equal to L-W. To obtain minimum size square devices, L' should therefore tend to zero, which is in practice impossible. Ideal GAA devices with same front and back gate lengths would therefore exhibit L > W. The optimization of L' for given W and L is a crucial point to focus on in the future. However, our priority was neither to achieve excellent speed performance nor to obtain large scale integration, but well to study highly reliable and reproducible devices. Therefore, we have chosen for L', W and L the minimum drawing feature size, equal to 3µm. The minimum oversize of the cavity in our actual devices is hence quite large and reaches L_{ov} = W/2 = 1.5µm. Increasing parasitic capacitances and/or resistances at a reasonable expense of silicon area is however useful in some applications, for instance to enhance the hardness of static memories irradiated by heavy particles (SEU hardness) as will be shown in Chapter VII.

Another limitation of the GAA process is that L'', the length of the free-standing portion of silicon given by (1-1), could not be increased above 6µm. Longer silicon bars could mechanically break when the cavity is opened and is not yet filled by the back polysilicon gate. As a consequence, with L' = 3µm, L should be smaller than 6µm, and W, smaller than 3µm. The minimum feature size of our technology being 3µm, devices with width-to-length ratios smaller(larger) than 0.5(unity) are designed by arranging several separated minimal square transistors in series(parallel). If the minimum device dimensions could be scaled below 3µm, width-to-length ratios smaller than 0.5 could be easily obtained by shrinking W. However, since devices with no overlap of the back gate should be designed with L > W, the drawback of having to place several individual transistors in parallel to increase the driving capability could not be overcome, even with a scaled technology.

When placed in parallel, individual silicon bars are separated by 5µm in order to allow correct mesa definition and good polysilicon filling of the cavity (Figure 1.8, left). On the other hand, when devices are placed in series, their individual gates are spaced by 6µm (Figure 1.8, right). This layout rule ensures that the different cavities do not overlap so that the silicon bars are regularly sustained by 3µm-long regions where the buried oxide is not removed. Consequently, poor compactness is achieved when GAA circuits are compared to conventional SOI realizations.

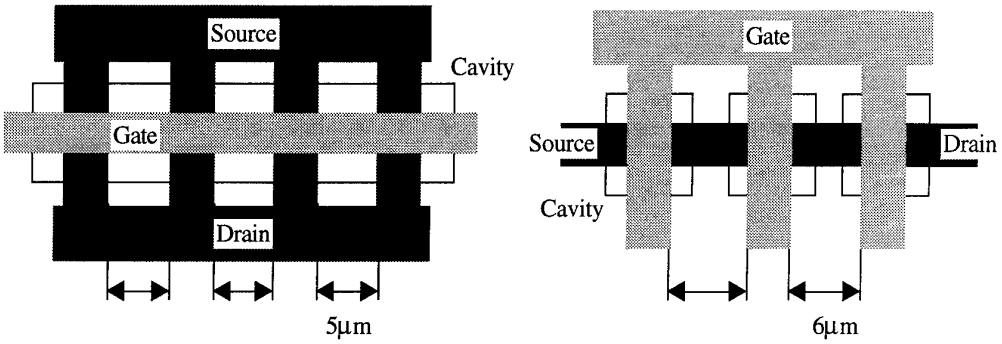

Figure 1.8: Minimum spacing between minimum size GAA devices placed in parallel (left) or in series (right).

Finally, we have to mention that the back-gate-to-substrate capacitance is increased in the GAA structure compared to the regular SOI technology because a thin gate oxide layer only separates the back-gate from the substrate.

3. Scaling

When the dimensions of bulk devices penetrate into the deep-submicrometer regime, the threshold voltage should be increased to prevent a punchthrough current to flow. This is usually performed by increasing the channel doping which, in turn, leads to detrimental effects such as reduced mobility and high junction capacitances. In fully-depleted SOI transistors, the high channel doping can be reduced because horizontal leakage is better controlled by the vertical front-to-back gate structure. Double-gate FETs are even more immune to short channel effects than FD SOI devices (for the same channel thickness), because the backside conducting layer further screens the source and drain fields away from the channel [28]. Hence, it is believed that double-gate transistors can be scaled down to the shortest dimensions [29,30,31]. The ultimate scaling of the silicon film thickness t_{si}, the gate oxide thickness t_{ox}, the device length L and the device width W is not only governed by physical limits but also by technological difficulties. We will discuss how far double-gate devices could be scaled down using the GAA technology.

The gate oxide thickness cannot be decreased below 3nm in order to prevent tunneling. Using a Re-Oxidized Silicon Island Edge (ROSIE) isolation for SOI devices, which is quite similar to the oxidation involved in the GAA process to round off the corners of the silicon island, a 8.4nm-thick gate oxide has been reported [32]. We expect that similar thicknesses could therefore be achieved for the gate oxide in GAA and should be suitable for low voltage applications.

Scaling the silicon film, the threshold voltage is much more sensitive to the t_{si} non-uniformity. Three other effects finally limit the t_{si} scaling around 5nm: quantum-mechanical uncertainty of the threshold voltage [31,33], excessive source/drain resistance and statistical fluctuations of the threshold voltage due to the discrete position of dopants. The quantum-mechanical limit cannot be overcome. Several options exist to reduce source/drain resistances such as recessed channel [34], raised source/drain [35], lateral

contact structure [36], selective tungsten deposition [37], and very thin silicide on source/drain regions [38]. Finally, statistical doping-related fluctuations can be suppressed by controlling the threshold voltage in adjusting the gate work function, the channel remaining undoped [39]. Those solutions involve so complex processes that, usually, decreasing t_{si} beyond 30nm brings more disadvantages than improvements in device performance. We suspect that the GAA process could even not achieve this 30nm lower limit for t_{si}. First of all, we should indeed keep in mind, that the thinner the silicon film, the more probable the mechanical fracture of the free-standing silicon bar after the cavity etching. This constraint is nevertheless relaxed when both length and width of the device are scaled down. A more serious problem lies in the particularly large source/drain series resistances linked to the overlap L_{ov} of the bottom gate. Furthermore, we will soon come to the point that a too small t_{si} limits the scaling of W.

Monte Carlo simulations of double-gate structures [31] have been presented where, with t_{ox} = 3nm and t_{si} = 5nm, the gate length can be scaled down to 30nm while still causing at most 0.08V threshold voltage roll-off for a 30% decrease of L below its nominal value. Theoretical investigations have shown that good subthreshold characteristics are obtained if the gate length is maintained longer than the so-called natural length λ, by a factor depending on the application. In [40], Suzuki *et al.* keep $\alpha = L/2\lambda$ above 3 to alleviate punchthrough. In double-gate structures, λ is given by [40,41]:

$$\lambda = \sqrt{\left(\frac{\varepsilon_{si} t_{si} t_{ox}}{2\varepsilon_{ox}}\right)\left(1+\frac{\varepsilon_{ox} t_{si}}{4\varepsilon_{si} t_{ox}}\right)}$$

when the punchthrough is assumed to flow along the middle of the film. On the other hand, stating that the punchthrough current flows at the surface, λ is minimum [42]:

$$\lambda = \sqrt{\left(\frac{\varepsilon_{si} t_{si} t_{ox}}{2\varepsilon_{ox}}\right)} \qquad (1\text{-}3)$$

ε_{si} and ε_{ox} are the permittivity constants of silicon and silicon dioxide, respectively.

Following this scaling rule, the doping concentration N_A should not be increased in order to avoid punchthrough. However, it has also been shown that increasing the doping shifts the punchthrough current from the center of the film towards the surface [43], hence minimizing λ and reducing short channel effects. On the contrary, the dominant punchthrough path moves from surface to center with increased drain bias and reduced channel length [43]. The dependence on the silicon film thickness is more complicated and depends on the other device parameters and biases. It has also been demonstrated that λ takes the minimum value (1-3) in double gate MOSFETs with N^+ polysilicon for the back gate and P^+ polysilicon for the front gate [44,45,46,47]. With realistic values t_{ox} = 10nm and t_{si} = 30nm, 21nm < λ < 24nm and L could be shrunk down to 0.15µm. An optimized double-gate process could therefore pushed further state-of-the-art 0.25µm and 0.18µm technologies without requiring extreme scaling of t_{ox} and t_{si}. Unfortunately, using the GAA process, an early limitation arises from the device width. W and L must indeed be scaled simultaneously in order to maintain the L_{ov}/L ratio

within acceptable values and, in thin films, narrow-channel effects dominate short-channel effects [48].

Narrow-channel effects become significant as soon as the channel width is of the same order of magnitude than the thickness of the depletion region under the gate oxide. A decrease of the channel width leads to an increase (conventional narrow-channel effect) or a decrease (inverse narrow-channel effect) of the threshold voltage depending on the gate recess, the doping concentration, the bias, the fixed oxide charges [49], the mode of operation of the transistor (inversion-mode or accumulation-mode) [50], and the silicon film thickness [48]. When W is still above 1μm, it is expected that the ROSIE isolation, which smoothes out the corner of the silicon island, lessens the negative threshold voltage shift compared to what should be obtained with a simple mesa structure [32]. However, it becomes extremely difficult to control the threshold voltage when W becomes comparable to the total length of the two bird's-beaks formed by the ROSIE re-oxidation [32]. This bird's beak punchthrough arises with W between 1μm and 0.6μm, and excessive thinning of silicon film thickness causes the device to fail much earlier [32,48]. In GAA, this narrow punchthrough effect will therefore probably limit W (and L if no overlap of the back-gate below the source/drain regions is allowed) to the micron range, and t_{si} to the 50nm-70nm range.

4. Electrical characterization

The previously described realization of GAA devices is quite exotic at first sight. Nevertheless, beyond the singularity of the GAA structure, lies a much more wide and up-to-date interest for the double-gate device family in general. As we have seen, double-gate SOI MOSFETs have been launched into the forefront of research because they are thought to be the limits of scaling. They also provide a nearly ideal coupling between gate and body potential from both sides of the silicon film. Numerous advantages of double-gate MOS transistors over regular single-gate fully depleted SOI devices have been reported or predicted by numerical simulations [51,52,53], such as a better subthreshold slope and lower leakage currents, higher current and transconductance, kink effect suppression and increased avalanche voltage. Using exactly the same process than regular CMOS SOI except for one additional masking step, GAA transistors provide a unique opportunity to compare significantly single and double-gate device performance. Some basic results are provided below.

The polysilicon gate of both n- and p-channel transistors is doped with phosphorus (N^{++}). Adequate threshold voltages are obtained in both cases with a rather heavily doped P^+ channel ($N_A \cong 10^{17}cm^{-3}$ in n-channels and $N_A \cong 6\times10^{16}cm^{-3}$ in p-channels). As a consequence, n-channel devices are inversion-mode, while p-channel devices work in accumulation regime [54]. N-type SOI measurements have been performed with the back interface near inversion (V_{BS} = 23V) so that they represent the best performance that FD SOI devices can achieve. On the other hand, when working with p-channel SOI transistors, the back-gate voltage has been adjusted to obtain the same threshold voltage than in p-type GAA devices (V_{BS} = 7V).

The drain current I_D of 60μm × 3μm SOI and GAA devices (realized in both technologies by the parallel combination of twenty minimum size square transistors) is plotted in Figure 1.9 as a function of the gate voltage overdrive (V_{GS}-V_{th}, with V_{GS} and V_{th} the gate and threshold voltages respectively), in linear operation (V_{DS} = ±0.1V with V_{DS} the drain voltage, the source terminal being grounded). The subthreshold slope S is steepest in the GAA structure than in the SOI counterpart: in p-channel devices, S = 0.064V/dec in GAA and only 0.078V/dec in SOI; in n-channel transistors, S = 0.062V/dec in GAA against 0.068V/dec in SOI. In Chapter II, it will be demonstrated (in the case of n-channel devices) that the strong gate-to-channel coupling brings the GAA subthreshold slope very close to the ideal value of 0.059V/dec. Any increase above this value is due to the presence of interface states. The n-channel drain current presents, below threshold, an unexpected bump related to an early conduction at the edges of the device. The different behavior of this edge conduction in GAA and SOI devices will be detailed in Chapter V. As already mentioned, this bump could be reduced by proper processing that should consist in increasing the doping concentration of the edges to locally raise the threshold voltage.

Above threshold, the current is larger in GAA transistors than in SOI devices at same bias and device dimensions. The current should indeed be at least a factor of two larger in GAA because conducting layers are formed at both the front and back interfaces. The ratio R between the GAA current and twice the SOI current ($R = I_{D,GAA}/2I_{D,SOI}$) should therefore be at least equal to unity. R is plotted in Figure 1.10 as a function of the gate voltage overdrive. It is clear that, above threshold, R exceeds unity. This current improvement can be explained by the wider spread of the carriers in the volume of the GAA film where they benefit from a larger mobility than at the surface. This point will be discussed in Chapter II. In the subthreshold region, R strongly increases in pMOS and confirms that no edge conduction affects p-channel devices. On the other hand, in n-channel devices, R tends to zero in the subthreshold region, indicating that the edge conduction appears earlier in the SOI structure than in the GAA counterpart. Both devices have, nevertheless, approximately the same geometry and doping concentrations.

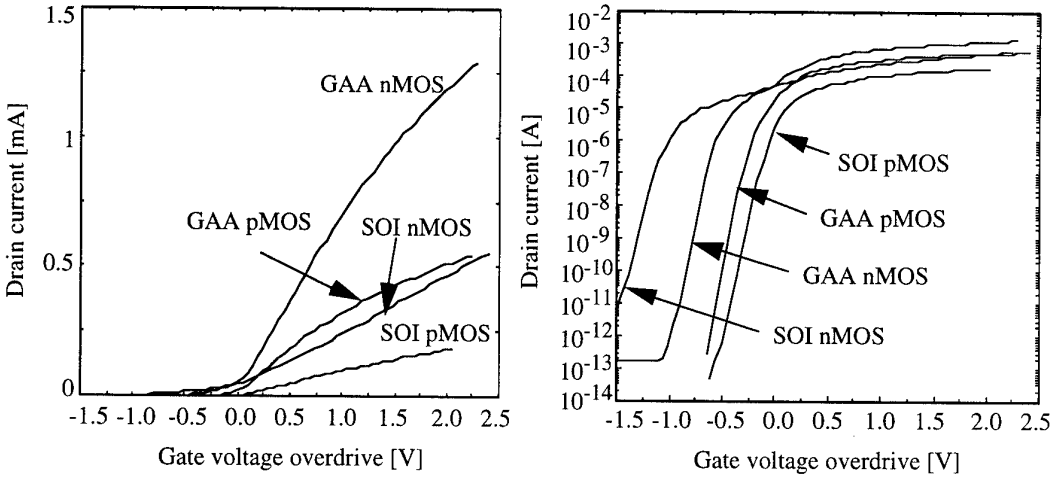

Figure 1.9: Drain current as a function of the gate voltage overdrive in linear operation (V_{DS} = ±0.1V) for 60μm × 3μm n- and p-channel SOI and GAA devices. Linear (left) and logarithmic (right) plots.

The transconductance $g_m = (\partial I_D / \partial V_{GS})$ is presented in Figure 1.11 as a function of the gate voltage overdrive. The improved volume conduction is again responsible for the observed enhancement of the transconductance by a factor of more than two between single- and double-gate structures. The ratio between the maximum g_m of SOI and GAA devices is found in the threshold region and is equal to 3.2 in nMOS and to 3.4 in pMOS.

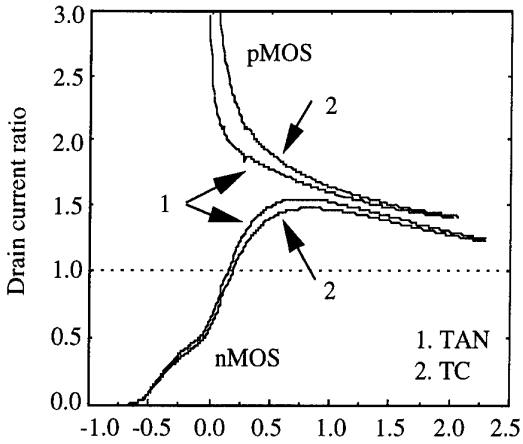

Figure 1.10: Drain current ratio ($I_{D,GAA}/2I_{D,SOI}$) as a function of the gate voltage overdrive in linear operation (V_{DS} = ±0.1V) for 60µm × 3µm n- and p-channel SOI and GAA devices.

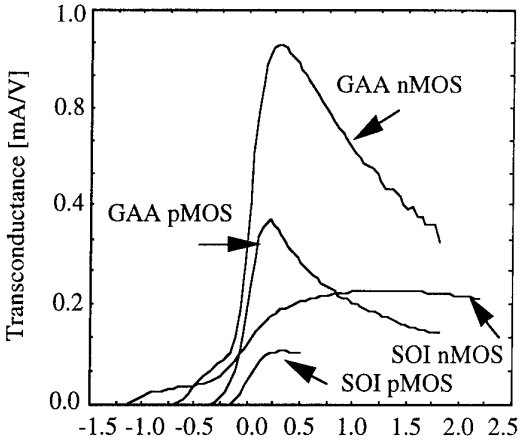

Figure 1.11: Transconductance as a function of the gate voltage overdrive in linear operation (V_{DS} = ±0.1V) for 60µm × 3µm n- and p-channel SOI and GAA devices.

Figures 1.12 and 1.13 allow to compare nMOS and pMOS GAA and SOI drain currents as a function of the drain voltage with the gate bias as parameter. In addition to their larger drive current capability (see graph scales), the double-gate structure exhibits flatter curves in saturation operation. This is especially remarkable in inversion-mode n-channel devices and reveals lower parasitic body effects [55] such as the kink effect.

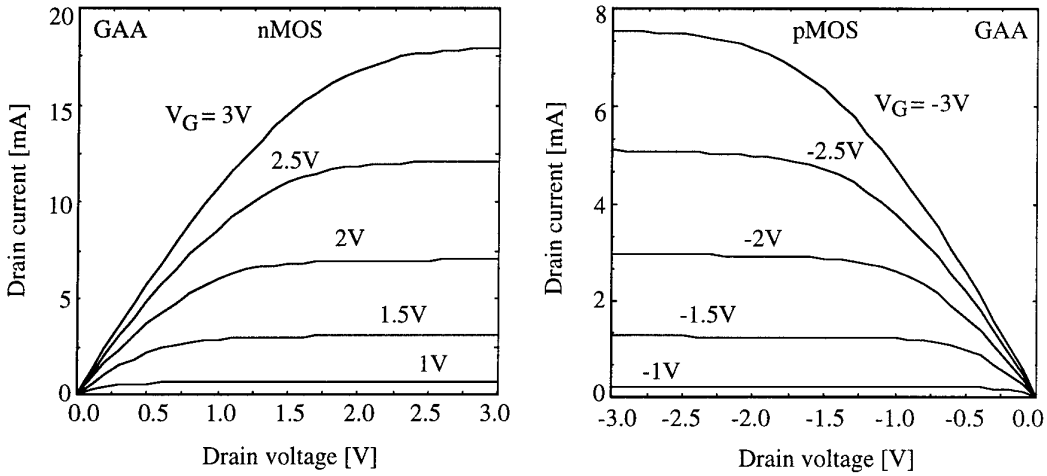

Figure 1.12: Drain current as a function of the drain voltage with the gate voltage as parameter (varying from 0V by steps of ±0.5V) in 60µm × 3µm n- (left) and p-channel (right) GAA devices.

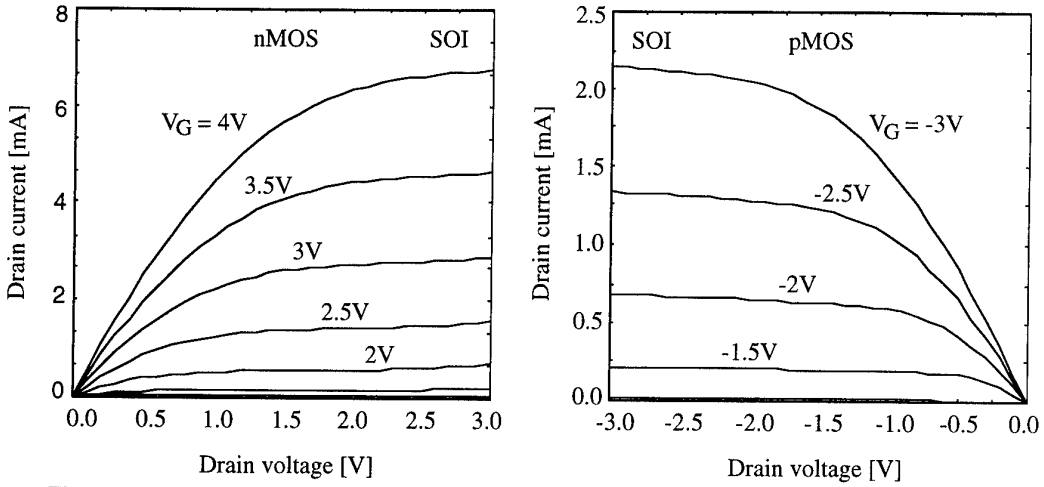

Figure 1.13: Drain current as a function of the drain voltage with the gate voltage as parameter (varying from 0V by steps of ±0.5V) in 60µm × 3µm n- (left) and p-channel (right) SOI devices.

Figure 1.14 shows, for both device types, the equivalent Early voltage V_{EA}. V_{EA} is defined as $V_{EA} = I_{D0}/g_D$ with the output conductance $g_D = (\partial I_D/\partial V_D)|_{I_{D0}}$ and I_{D0} chosen such that g_D is maximum. V_{EA} is around 30...100V in GAA devices depending on the operating conditions and only around 25V in SOI independently on the gate voltage. The large Early voltage of the GAA structure arises because of the reduced extension of the drain-controlled channel region. This crucial improvement is very important for analog applications since the intrinsic voltage gain of a transistor is proportional to V_{EA}. This advantage will be confirmed at high temperature operation (Chapter III) and even subsists under total-dose irradiation (Chapter V).

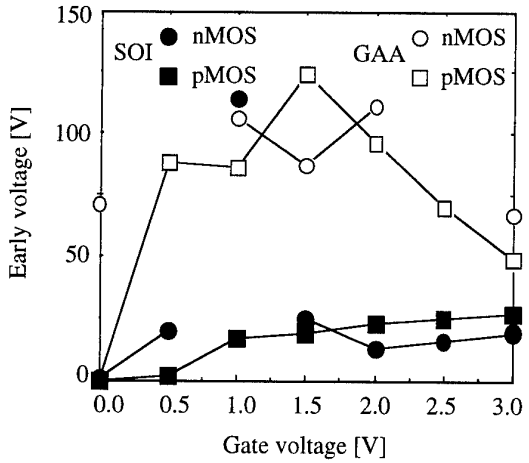

Figure 1.14: Early voltage as a function of the gate voltage in 60µm × 3µm n- and p-channel GAA and SOI devices.

The breakdown voltage V_{BD} is depicted in Figure 1.15 as a function of the drawing length in 3µm-wide GAA devices and 20µm-wide SOI transistors. As expected from the strong control of the gate on the body potential, the breakdown voltage is larger in GAA than in SOI n-channel devices. V_{BD} is respectively around 4.4V and 2.6V and is defined by the invariant point of the I_{DS}-V_{DS} curves when V_{GS} is swept in the subthreshold region. On the contrary nevertheless, V_{BD} measured in the subthreshold region of

accumulation-mode p-channel devices is smaller (in absolute value) in GAA (-5.5V) than in SOI (-6.2V) [56] but still much larger than in inversion-mode transistors. V_{BD} is here defined by the onset of the gate current (I_G = 2.5pA) which is related to hot-carrier injection in the gate oxide and hence to avalanche multiplication.

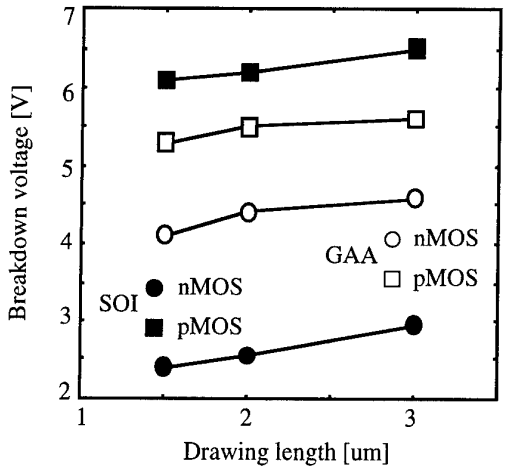

Figure 1.15: Breakdown voltage as a function of drawing length in n- and p-channel 3µm-wide GAA and 20µm-wide SOI devices.

5. Conclusions

The fabrication process of the Gate-All-Around (GAA) device, which belongs to the double-gate device family, was presented. The process is very similar to the regular SOI process except that cavities are locally etched in the buried oxide. These holes allow the active silicon bars to be totally wrapped in the thin gate oxide layer and in the polysilicon gate. When the cavity etching is not optimized, GAA devices present large parasitic source/drain resistances as well as large parasitic capacitances which prevent high frequency operation. We showed that the device dimensions could be shrunk down to the micron range but probably not beyond. Finally, numerous electrical advantages, such as high current and transconductance, nearly ideal subthreshold slope and small output conductance were measured. These benefits arise from the very tight (nearly ideal) control of the gate on the body potential and make GAA devices especially attractive for low voltage or low power operation. The following chapter will propose theoretical demonstrations of these advantages in the case of long-channel nMOSFETs.

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Chapter II: Modeling of n-channel inversion-mode GAA MOSFETs in linear regime

The excellent electrical characteristics of double-gate MOS transistors rely on the concept of volume inversion. Optimum gate-to-body coupling arises symmetrically from both sides of the silicon film. As a consequence, the minority carriers are no longer confined near the surface, but are found across the whole film. The resulting quite flat potential distribution is unique and different from that in bulk and single-gate SOI MOSFETs so that classical analyses cannot be used. It is then necessary to develop specific and reliable analytical models in order to understand and easily optimize the electrical properties of these double-gate transistors. Different expressions have been previously established for the threshold voltage and the drain current in the subthreshold and strong inversion regions. Unfortunately, they do not apply to all regimes and are especially inappropriate in the weak inversion region. For example, models based on the strong inversion approximation [1,2,3] are suitable at high gate voltage but are inadequate near threshold, because a current flows in highly-doped double-gate devices even if no part in the film has reached strong inversion. On the other hand, the approximation proposed for conventional SOI devices [4,5], that uses a constant potential distribution across the film, yields only reasonably good results in the subthreshold region when applied to double-gate structures [6,7].

The condition to obtain a model continuously valid and accurate from subthreshold to strong inversion regime is to take simultaneously into account both the dopant impurity charges and the minority carrier concentration. This excludes the charge sheet approximation [8,9,10]. Several one-dimensional (1D) analytical models, focusing on long ($L \geq 0.5\mu m$) n-channel devices in linear operation, will now be presented and compared. They significantly outperform previous studies in terms of physical insight on the volume inversion mechanisms and range of validity.

Not only the potential distribution is derived but also the current, the transconductance, the threshold voltage and the subthreshold slope. Starting from implicit expressions, judicious simplifications are proposed and discussed to obtain analytical formulations. Simultaneously, the advantages of the double-gate structure over conventional SOI devices are reviewed and discussed.

1. Body potential distribution

Figure 2.1 shows a schematic cross-section of a double-gate MOS transistor. The x-axis is perpendicular to the surface and x = 0 refers to the center of the film. The y-axis runs from source to drain. We assume that the device channel region is fully depleted, which implies that the silicon film thickness t_{si} is much smaller than twice the maximum extend of the depletion region x_{dmax}. Using the strong inversion approximation, $x_{dmax} = 2\sqrt{(4\varepsilon_{si}\phi_F/qN_A)}$ where ϕ_F is the Fermi potential and q is the electronic charge. Furthermore, we assume a uniform doping density N_A which is a very acceptable approximation for ultra-thin film devices.

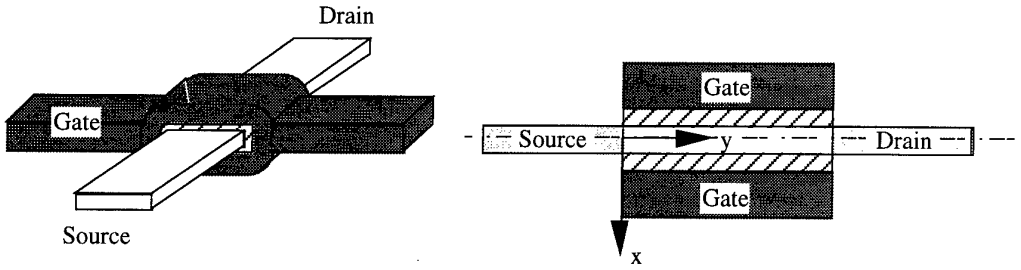

Figure 2.1: Three-dimensional view and longitudinal cross-section of a GAA transistor.

Assuming that the minority carrier concentration is almost uniform, by comparison with bulk or thick SOI devices, and is of the same order of magnitude than the fixed charge density, the distinction between a depleted region in the body and strong inverted layers at the Si/SiO_2 interfaces is no longer possible. Therefore, the classical approximation $|\rho(x)| = \max\{qN_A, qn(x), qp(x)\}$ of the space charge density $\rho(x) = q(p(x)-n(x)-N_A)$ is clearly not adequate. In other words, the Poisson equation can neither be reduced to the depletion approximation (D):

$$\frac{d^2\phi(x,y)}{dy^2} + \frac{d^2\phi(x,y)}{dx^2} = \frac{qN_A}{\varepsilon_{si}} \tag{2-1}$$

nor to the strong inversion model (SI) [11]:

$$\frac{d^2\phi(x,y)}{dy^2} + \frac{d^2\phi(x,y)}{dx^2} = \frac{qn(x,y)}{\varepsilon_{si}} \tag{2-2}$$

The problem is that, up to now, the Poisson equation, where only the majority carrier concentration is omitted, has not be solved satisfactorily for GAA devices:

$$\begin{aligned}\frac{d^2\phi(x,y)}{dy^2} + \frac{d^2\phi(x,y)}{dx^2} &= \frac{q}{\varepsilon_{si}}\left[N_A + n(x,y)\right] \\ &= \frac{q}{\varepsilon_{si}}\left[N_A + \frac{n_i^2}{N_A} e^{\frac{q}{kT}[\phi(x,y)-V(y)]}\right]\end{aligned} \tag{2-3}$$

The potential $\phi(x,y)$ is referred to the neutral region of the equivalent bulk MOS transistor. V(y) is the electron quasi-Fermi potential depending on the voltage applied to

the channel between source and drain, independently of x. n_i is the intrinsic carrier concentration. Other notations have their usual meaning. In ohmic operation (small drain to source bias), the variations along the y-direction may be neglected. With same source and drain voltages, $V_S \approx V(y) \approx V_D$, the model restricts to a 1D analysis. Since the double-gate transistor is a three-terminal device with no influence of the substrate bias, the source voltage V_S can be set to zero without loss of generality. Hence, we further assume that $V(y) = 0$.

The boundary conditions of the problem are the symmetry of the structure around the center of the film $x = 0$ (Figure 2.1) and Gauss' Law at the Si/SiO_2 interface:

$$\frac{\varepsilon_{si}}{C_{ox}} E_S = V_G - V_{FB} - \phi_S \tag{2-4}$$

with V_G the gate voltage, E_S the surface electric field, ϕ_S the surface potential, C_{ox} the capacitance associated to the gate oxide layer and V_{FB} the flat-band voltage. The interface state density is omitted.

Including both depleted and induced charges, equation (2-3) is valid in all bias regions but no analytical integration can be found without introducing a local approximation of $n(x,y) = n(x)$.

1.1. Basic moderate inversion center model - MIC0

The first simplest model replaces the electron concentration by its value n_0 at the center of the film:

$$\frac{d^2\phi(x)}{dx^2} = \frac{q(N_A + n_0)}{\varepsilon_{si}} = \frac{q}{\varepsilon_{si}}\left(N_A + \frac{n_i^2}{N_A} e^{\frac{q}{kT}\phi_0}\right)$$

with ϕ_0 the mid-film potential. This constant potential approximation CP [6,7] results in the following electric field and potential distributions:

$$\begin{aligned} E(x) &= -\frac{q(N_A + n_0)}{\varepsilon_{si}} x \\ \phi(x) &= \frac{q(N_A + n_0)}{\varepsilon_{si}} \frac{x^2}{2} + C_1 x + C_2 \end{aligned} \tag{2-5}$$

Constants C_1 and C_2 are fixed by boundary conditions:

$$C_1 = 0 \text{ and } C_2 = V_G - V_{FB} - \frac{q(N_A + n_0)}{\varepsilon_{si}} \frac{t_{si}}{2}\left(\frac{t_{si}}{4} + \frac{\varepsilon_{si}}{C_{ox}}\right)$$

Finally, the last unknown parameter ϕ_0 is given as a function of the gate voltage by solving the implicit so-called "self-consistency" equation obtained when evaluating (2-5) at the middle of the film:

$$\phi_0 = C_2(\phi_0)$$

1.2. Improved moderate inversion center model - MIC2

Taking into account higher-order terms of the Taylor development of n(x) around the center of the film should improve the previous model. The first order term drops owing to the symmetry of the structure. Introducing the second order term tends to increase the electron concentration present beneath the surface. From (2-3), it becomes:

$$\frac{d^2\phi(x)}{dx^2} = \frac{q}{\varepsilon_{si}}\left(N_A + \frac{n_i^2}{N_A}e^{\frac{q}{kT}\phi_0}\left[1 + \frac{q}{kT}\frac{d^2\phi(x)}{dx^2}\bigg|_0 \frac{x^2}{2}\right]\right)$$

$$= \frac{q}{\varepsilon_{si}}\left(N_A + n_0\left[1 + \frac{q}{kT}\frac{q}{\varepsilon_{si}}(N_A + n_0)\frac{x^2}{2}\right]\right)$$

Related electric field and potential distributions are:

$$E(x) = -\frac{qn_0}{\varepsilon_{si}}\frac{q}{kT}\frac{q(N_A + n_0)}{\varepsilon_{si}}\frac{x^3}{6} - \frac{q(N_A + n_0)}{\varepsilon_{si}}x$$

$$\phi(x) = \frac{qn_0}{\varepsilon_{si}}\frac{q}{kT}\frac{q(N_A + n_0)}{\varepsilon_{si}}\frac{x^4}{24} + \frac{q(N_A + n_0)}{\varepsilon_{si}}\frac{x^2}{2} + C_1x + C_2$$

with $C_1 = 0$ and

$$C_2 = V_G - V_{FB} - \frac{q(N_A + n_0)}{\varepsilon_{si}}\frac{t_{si}}{2}\left(\frac{t_{si}}{4} + \frac{\varepsilon_{si}}{C_{ox}}\right) - \frac{qn_0}{\varepsilon_{si}}\frac{q}{kT}\frac{q(N_A + n_0)}{\varepsilon_{si}}\frac{t_{si}^3}{48}\left(\frac{t_{si}}{8} + \frac{\varepsilon_{si}}{C_{ox}}\right)$$

The mid-film potential is still extracted from the implicit self-consistency condition:

$$\phi_0 = C_2(\phi_0)$$

1.3. Moderate inversion surface model - MIS

The idea is to use a first order development of $\phi(x)$ around the surface of the film. For $(-t_{si}/2) \le x \le 0$, (2-3) becomes:

$$\frac{d^2\phi(x)}{dx^2} = \frac{q}{\varepsilon_{si}}\left(N_A + \frac{n_i^2}{N_A}e^{\frac{q}{kT}\left[\phi_S - \left(\frac{t_{si}}{2}+x\right)E_S\right]}\right) = \frac{q}{\varepsilon_{si}}\left(N_A + n_S e^{\frac{-q}{kT}\left(\frac{t_{si}}{2}+x\right)E_S}\right)$$

where n_S is the surface electron concentration. Below threshold, the potential is so flat that any tangent should correctly approximate the potential distribution. Above threshold, this model, on the contrary to previous approaches, favors the surface of the silicon film where the electrons pile up when the gate voltage increases. After a double integration with the previously mentioned boundary conditions, we obtain:

$$E(x) = -\frac{qN_A}{\varepsilon_{si}}\left(\frac{t_{si}}{2}+x\right) - C_1 + \frac{q}{\varepsilon_{si}}\frac{kT}{q}\frac{n_S}{E_S}e^{\frac{-q}{kT}\left(\frac{t_{si}}{2}+x\right)E_S}$$

$$\phi(x) = \frac{qN_A}{\varepsilon_{si}}\frac{\left(\frac{t_{si}}{2}+x\right)^2}{2} + C_1\left(\frac{t_{si}}{2}+x\right) + C_2 + \frac{q}{\varepsilon_{si}}\left(\frac{kT}{q}\right)^2\frac{n_S}{E_S^2}e^{\frac{-q}{kT}\left(\frac{t_{si}}{2}+x\right)E_S} \quad (2\text{-}6)$$

with $$C_1 = \frac{q}{\varepsilon_{si}}\left(\frac{kT}{q}\frac{n_S}{E_S}e^{\frac{-q}{kT}\frac{t_{si}}{2}E_S} - N_A\frac{t_{si}}{2}\right) = \frac{q}{\varepsilon_{si}}\frac{kT}{q}\frac{n_S}{E_S} - E_S \quad (2\text{-}7)$$

and $$C_2 = \phi_S - \frac{q}{\varepsilon_{si}}\left(\frac{kT}{q}\right)^2\frac{n_S}{E_S^2}$$

The left and right hand sides of the self-consistency condition (2-7) result from the evaluation of E(x) at the middle and at the surface of the film, respectively. Relationship (2-7), combined with Gauss' Law (2-4), allows the computation of E_S, ϕ_S and n_S as a function of gate voltage:

$$E_S + \frac{kT}{q}\frac{qn_S}{\varepsilon_{si}E_S}\left(e^{-\frac{q}{kT}\frac{t_{si}}{2}E_S} - 1\right) - \frac{qN_A}{2C_{si}} = 0$$

$$n_S = \frac{n_i^2}{N_A}e^{\frac{q}{kT}\phi_S} \quad (2\text{-}8)$$

$$\frac{\varepsilon_{si}}{C_{ox}}E_S = V_G - V_{FB} - \phi_S$$

with C_{si} the capacitance associated to the silicon film.

1.4. Discussion

In Figure 2.2, the evolution of the surface and mid-film potentials as a function of the gate voltage, obtained by different models (D, SI, MIC0, MIC2 and MIS), are compared and confronted to two-dimensional Medici [12] simulations. The set of parameters corresponds to devices processed in our clean room with N^+ polysilicon gates. Since the work function difference ϕ_{ms} between the n-type gate and the p-type channel is strongly negative, a large film doping concentration ($N_A = 10^{17}cm^{-3}$) is necessary to compensate for the negative flat-band voltage (V_{FB} = -1V). The resulting positive threshold voltage is around 0.7V.

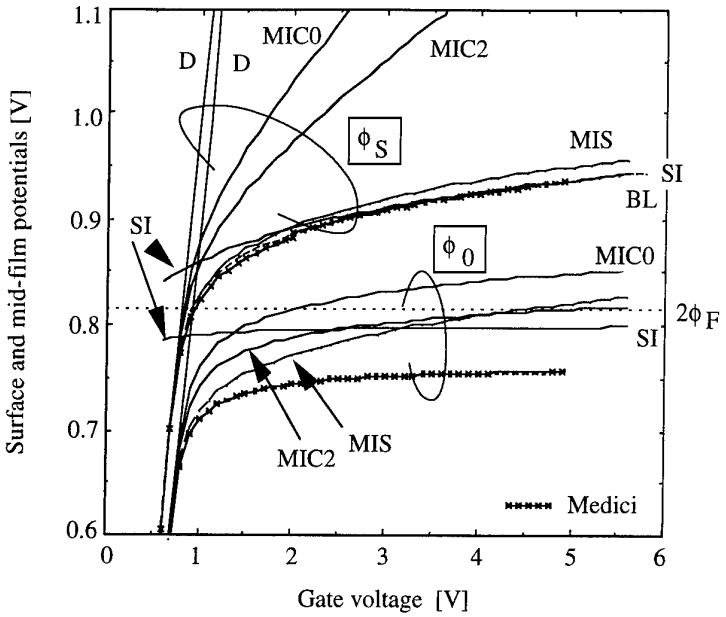

Figure 2.2: Surface and mid-film potential distributions provided by different analytical models: t_{si} = 75nm, t_{ox} = 55nm, $N_A = 10^{17}cm^{-3}$, V_{FB} = -1V, and V_{th} = 0.72V.

As far as the estimation of the surface potential is concerned, the depletion approximation (D) is only suitable in the subthreshold region where the potential distribution linearly shifts with the gate voltage. The strong inversion approximation (SI) becomes only very accurate at a gate voltage of more than 2V (gate voltage overdrive V_G-V_{th} > 1V). In the intermediate region from subthreshold to strong inversion regime (0.7V< ... <2V), both previous models fail because neither the depletion nor the induced charge can be neglected. In this so-called "weak inversion" region, moderate inversion center models (MIC0, MIC2) improve the depletion approximation because they introduce a saturation of the surface potential above threshold. The comparison of MIC0 and MIC2 nevertheless suggests that a very large number of higher order terms should be included in the approximation of n(x) to reach a correct accuracy for ϕ_S at large gate voltage. On the other hand, the moderate inversion surface model (MIS) is continuously highly accurate in the whole gate voltage range. This is a very good news since from ϕ_S will derive current, threshold voltage and transconductance. Much less crucial, is the accuracy of the different models around the center of the film. Contrarily to what could be expected, models involving an approximation of n(x) around x = 0, like the MIC2 model, fail to approximate ϕ_0. Again, the MIS model exhibits best performance up to V_G = 3V. Therefore the MIS model, that simply replaces the potential by its tangent at the surface of the film before integrating Poisson's equation, is very powerful.

The complete potential distribution across the film is shown in Figure 2.3, in the weak inversion region, for V_G = 1V. This figure highlights the inadequacy of all models except the MIS approach, which nearly perfectly follows the Medici reference spots.

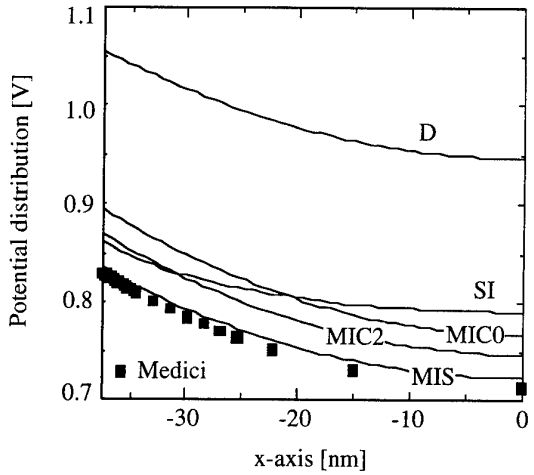

Figure 2.3: Potential distribution across the Si film for different analytical models at V_G = 1V: t_{si} = 75nm, t_{ox} = 55nm, N_A = $10^{17}cm^{-3}$, V_{FB} = -1V, and V_{th} = 0.72V.

In other to evaluate the robustness of the MIS model, another set of parameters corresponding to experimental devices reported in [13] is investigated in Figure 2.4. Those devices are realized with P^+ polysilicon gates. This change of the gate doping type ultimately results in a two orders of magnitude decrease in the film doping concentration (N_A = $10^{15}cm^{-3}$) in order to obtain about the same threshold voltage, here around 0.9V.

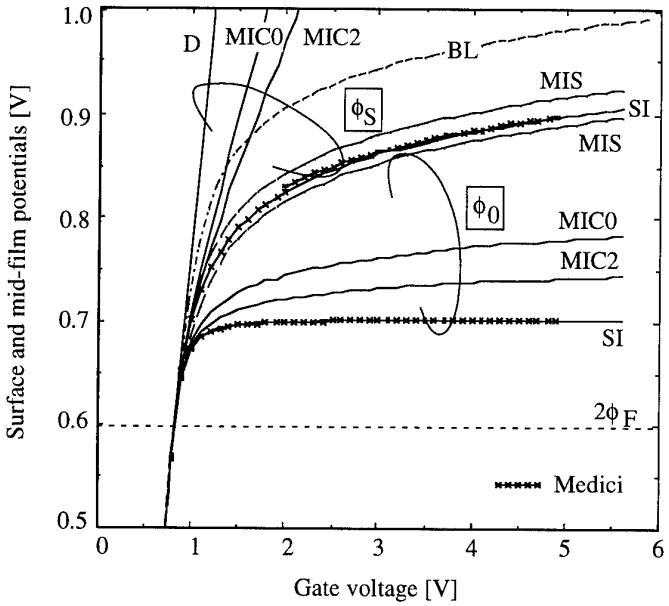

Figure 2.4: Surface and mid-film potential distributions provided by the different analytical models: t_{si} = 60nm, t_{ox} = 11nm, N_A = $1.5\times10^{15}cm^{-3}$, V_{FB} = 0.29V, V_{th} = 0.93V.

Figure 2.4 shows that, for low doped films, there is no gap between the regions of validity for D and SI approximations. The MIS model is nevertheless still welcome since it provides continuous accuracy of ϕ_S over the whole gate voltage range. No switching between different approximations (D and SI) is therefore required as a function of the operating conditions. However, the MIS model obviously fails to approximate ϕ_0, closely approached by the MIC0 and MIC2 models. As already mentioned, this is of less importance.

Figures 2.2 and 2.4 also highlight the impact of the doping concentration on the potential bending defined as the difference between surface and mid-film potentials ϕ_S-ϕ_0. Using the depletion approximation (2-1), suitable in the subthreshold region, it comes that ϕ_S-ϕ_0 is proportional to N_A:

$$\phi_S - \phi_0 = \frac{qN_A t_{si}^2}{8\varepsilon_{si}} = \frac{Q_D}{8C_{si}} \tag{2-9}$$

with Q_D the total depletion charge of the film. Therefore, below threshold, ϕ_S-ϕ_0 is non negligible (0.11V) in the high doping case (HD) of Figure 2.2 and perfectly negligible (1.1mV) in the low doping (LD) case of Figure 2.4. Hence, below threshold, the lower N_A, the flatter the potential and the larger the volume conduction.

In the strong inversion region, electrons pile up mainly at the surface and shield the bulk inversion charge. As a result, the mid-film potential increases more slowly than the surface potential and the potential bending increases. It could be shown from the SI approximation [1] that ϕ_0 is pinned at $2(kT/q)\ln\left((\pi/n_i t_{si})\sqrt{(kT/q)(2\varepsilon_{si}N_A/q)}\right)$ as soon as threshold is reached. In Figure 2.2 (HD case), ϕ_0 never exceeds the $2\phi_F$ value corresponding to strong inversion onset, while the surface potential saturates at about $2\phi_F + 5(kT/q)$, like in regular SOI devices. On the other hand, in Figure 2.4 (LD case), both ϕ_S and ϕ_0 are larger than $2\phi_F$ above threshold. This does not mean that the volume of the film contributes more largely to the global conduction in Figure 2.4 than in Figure 2.2, since the shape of the potential profile, rather than the position of the curve relatively to $2\phi_F$, determines whether conduction mostly occurs below the surface or in the volume. However, numerous simulations performed with same t_{ox} and t_{si} (which is not the case of Figures 2.2 and 2.4) show that lowering N_A always flattens the potential profile, not only below threshold, which is clear from (2-9), but also above threshold. Hence, reducing the doping concentration should profit to volume conduction. We will come back to this point later on.

In summary, the MIS model provides so far two advantages: it is the only reliable model in the weak inversion region, and it is continuously highly accurate in the whole gate voltage range. In a HD film (Figure 2.2), the slight increase of ϕ_S-ϕ_0 from subthreshold to strong inversion proceeds so smoothly that the weak inversion region extends over a wide gate voltage range. The former quality of the MIS model is hence the most remarkable. In a LD film, the weak inversion region nearly vanishes and the transition between subthreshold and strong inversion arises very abruptly. The latter property of the MIS model is hence very appreciated.

Finally, it should be noted that it is possible to extend the MIS model for non-symmetrical SOI devices, at least if the potential distribution is not monotonously decreasing across the film. Indeed, considering the point where the potential is minimum to split the transistor in two, the previous analysis remains valid in each part separately. The unknown splitting point is then obtained by imposing the continuity of the potential and the electric field.

2. Drain current

The current is proved to depend exclusively on the surface electric field which can be obtained directly from the models previously proposed which use two successive integrations of the Poisson equation. A second approach skips one integration of the Poisson equation and directly provides an expression of the surface electric field more accurate in weak inversion operation.

2.1. General expression of the current

The drain current is simply obtained by integration of the electron concentration from top to bottom gates. Although very interesting, the analysis of an adequate mobility model is out of the scope of this work. Therefore, we adopt a constant mobility μ_n throughout the film. At low drain bias, using (2-3), we obtain:

$$I_D = 2\frac{W}{L}V_{DS}\int_{\frac{-t_{si}}{2}}^{0} q\mu_n(x)n(x)dx \approx 2\frac{W}{L}V_{DS}\mu_n\int_{\frac{-t_{si}}{2}}^{0}\left(\varepsilon_{si}\frac{d^2\phi(x)}{dx^2} - qN_A\right)dx \qquad (2\text{-}10)$$

After integration, the surface electric field E_S directly appears:

$$I_D \approx \frac{W}{L}V_{DS}\mu_n\left(2\varepsilon_{si}E_S - qN_A t_{si}\right) \approx \frac{W}{L}V_{DS}\mu_n Q_N \qquad (2\text{-}11)$$

where Q_N is the total free charge, difference between the total charge ($2\varepsilon_{si}E_S$) and the depletion charge ($qN_A t_{si}$). The depletion charge is independent on V_G due to full depletion of the ultra-thin film device. The total charge is a function of the surface electric field only, owing to the fact that the electric field at the center of the symmetrical GAA structure equals zero.

2.2. From a double integration of the Poisson equation: the MIS model

E_S can be directly extracted from the self-consistency equation (2-8) of the MIS model, or can be provided by any other model previously mentioned (D, SI, MIC0, MIC2). The resulting Q_N is shown in Figure 2.5 in linear and logarithmic scales, for heavily doped (HD) devices. Medici simulations are presented as well (small crosses). The surface model (MIS) is, as expected, accurate in the whole gate bias range while the strong inversion model (SI) becomes only suitable at high gate voltage ($V_G > 1.5V$). The MIC0 and MIC2 models fail at large gate biases but also in the subthreshold region where they do not properly account for the non negligible potential bending (Figure 2.2).

The accuracy of the MIS model can be checked in Figure 2.6 which presents the absolute error $\varepsilon_a = \left[Q_{N,MIS} - Q_{N,Medici}\right]$ and the relative error $\varepsilon_r = \left(\varepsilon_a / Q_{N,Medici}\right)$ obtained when the MIS model is compared to Medici simulations. In the HD film case, ε_a is very small in the subthreshold region. At increasing V_G, ε_a steadily increases but ε_r continuously drops down to only 3% at $V_G = 1V$. Another method, labeled BL in Figure

2.6, is slightly more accurate than the MIS model in case of large doping concentration, and will now be presented.

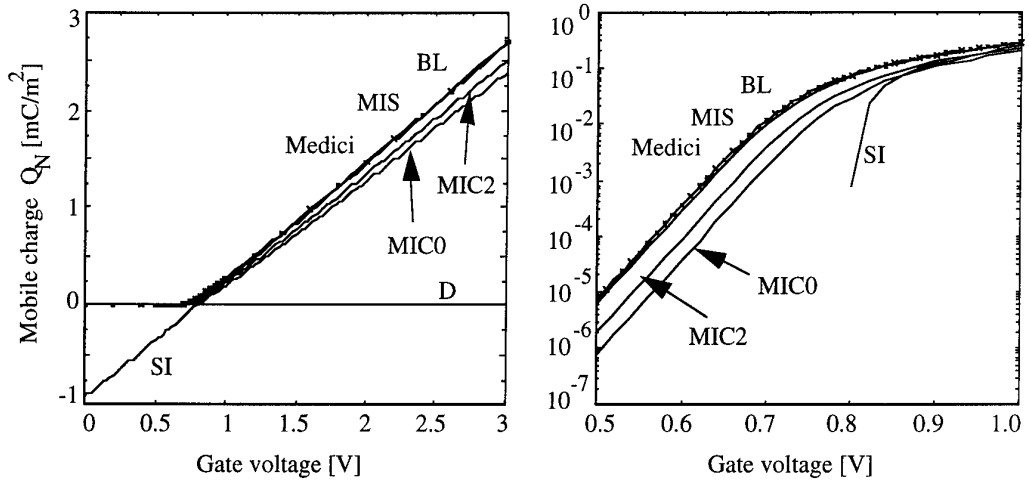

Figure 2.5: Mobile charge as a function of gate voltage for different analytical models.
HD film: t_{si} = 75nm, t_{ox} = 55nm, $N_A = 10^{17}cm^{-3}$, V_{FB} = -1V (N^+ poly gate), and V_{th} = 0.72V.

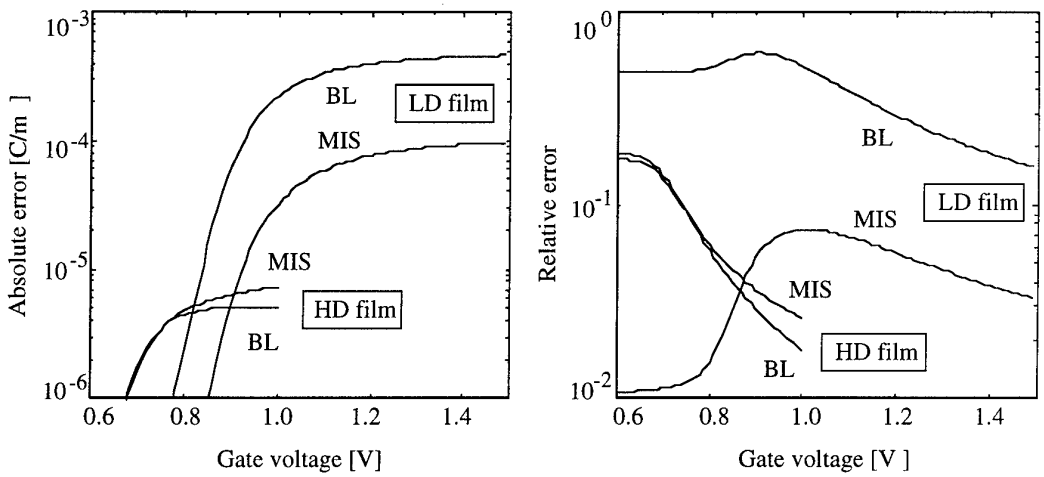

Figure 2.6: Absolute and relative errors of the drain current provided by MIS and BL models when compared to Medici simulations.
HD film: t_{si} = 75nm, t_{ox} = 55nm, $N_A = 10^{17}cm^{-3}$, V_{FB} = -1V (N^+ poly gate), and V_{th} = 0.72V,
LD film: t_{si} = 60nm, t_{ox} = 11nm, $N_A = 1.5\times10^{15}cm^{-3}$, V_{FB} = 0.29V (P^+ poly gate), V_{th} = 0.93V.

2.3. From a single integration of the Poisson equation: the BL model

The idea of the BL model, derived from the bulk analysis, is to skip one integration of the Poisson equation. Integrating (2-3) between the center and the surface of the film after multiplying both sides by 2[dϕ(x)/dx], yields:

$$E_S = \sqrt{\frac{2qN_A}{\varepsilon_{si}}}\sqrt{(\phi_S-\phi_0)+\frac{kT}{q}\frac{n_i^2}{N_A^2}e^{\left[\frac{q}{kT}\phi_S\right]}\left(1-e^{\left[\frac{-q}{kT}(\phi_S-\phi_0)\right]}\right)} \qquad (2\text{-}12)$$

Now, in fully-depleted double-gate SOI, contrarily to the bulk case where the potential at the limit of the depletion region is known to be zero, the mid-film potential ϕ_0 is unfortunately unknown. Figures 2.2 and 2.4 show that the potential bending (ϕ_S-ϕ_0) is constant in the subthreshold region and given by (2-9) from the depletion approximation. Since the linear term (ϕ_S-ϕ_0) is negligible in (2-12) compared to the exponential term, except in the subthreshold region where (2-9) is valid, it is justifiable to replace (ϕ_S-ϕ_0) by $Q_D/8C_{si}$. Using (2-4), E_S finally becomes an implicit function of the gate voltage only:

$$E_S = \sqrt{\frac{2qN_A}{\varepsilon_{si}}} \cdot \sqrt{\frac{Q_D}{8C_{si}} + \frac{kT}{q}\frac{n_i^2}{N_A^2} e^{\frac{q}{kT}\left[V_G - V_{FB} - \frac{\varepsilon_{si}}{C_{ox}}E_S\right]}\left(1 - e^{\frac{-q}{kT}\left[\frac{Q_D}{8C_{si}}\right]}\right)}} \qquad (2\text{-}13)$$

The resulting Q_N-V_G characteristic, called bulk-like (BL) curve, obtained when combining (2-13) and (2-11), nearly merges with the reference curve produced by Medici in the full gate voltage range of Figure 2.5. Figure 2.6 also shows that in HD film cases, the BL model provides a residual improvement to the MIS approximation, the relative error dropping now to 1.5% at V_G = 1V. Also, ε_a is very small, presents a peak around threshold and then decreases at large gate voltages. The threshold region is indeed the most critical region for the BL model because (ϕ_S-ϕ_0) is no longer strictly equal to (2-9) but is not yet negligible in (2-12). Using (2-4), the surface electric field obtained by the BL model yields an expression of the surface potential also very accurate as depicted in Figure 2.2. Unfortunately, the BL approach does not provide the potential distribution across the film simply because one integration of the Poisson equation has been skipped.

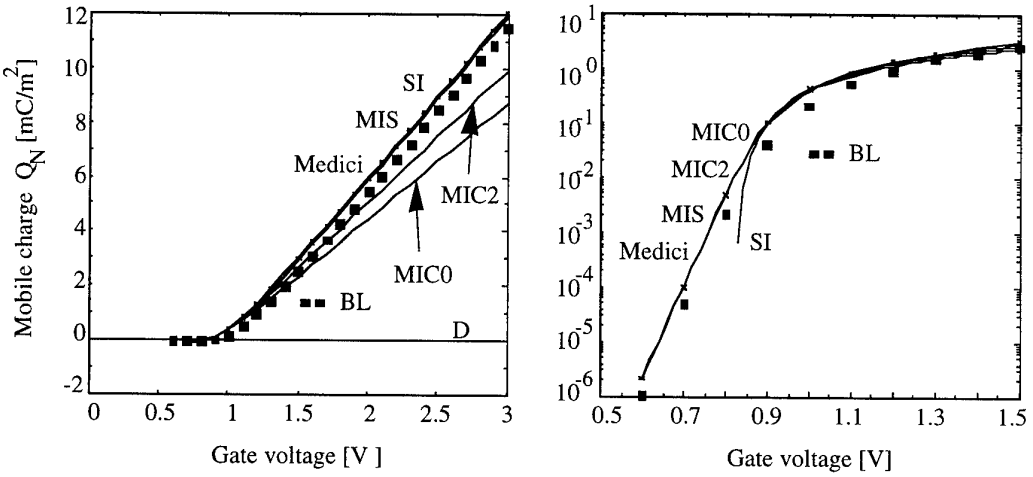

Figure 2.7: Mobile charge as a function of gate voltage for different analytical models.
LD film: t_{si} = 60nm, t_{ox} = 11nm, $N_A = 1.5\times10^{15}cm^{-3}$, V_{FB} = 0.29V (P^+ poly gate), V_{th} = 0.93V.

When the doping concentration of the film is reduced, the BL approximation produces a much larger error than the MIS model, as shown in Figure 2.6 (LD film case), and is clearly no longer acceptable at high gate bias. Indeed, the model presents a shift of both

the ϕ_S-curve in Figure 2.4 and the Q_N-curve in Figure 2.7. The reason is that a strong variation exists between the potential bending, very small, below threshold and, quite large, above threshold (Figure 2.4), so that, it is not adequate to insert the too small value (2-9) in the exponential term of (2-12) at high gate bias. On the other hand, Figure 2.6 shows that the accuracy of the MIS model is similar in HD and LD film cases with $\varepsilon_r <$ 10%, maximum obtained in the threshold region. Therefore, the BL model (2-13) should only be preferred to the MIS model (2-8) in situations where both fixed and induced charges contribute to determine the potential shape (large N_A). Putting Figures 2.2 and 2.4 in correspondence with Figure 2.6, it arises that the absolute error on the drain current increases with the potential bending above threshold independently of the chosen model (BL or MIS).

3. Threshold voltage

In spite of the fact that expression (2-11) giving the current is an implicit function of the surface electric field extracted from (2-8) or (2-13), it is possible to derive explicit expressions of the threshold voltage V_{th}. The usual definition of V_{th} is the gate voltage required to obtain $\phi_S = 2\phi_F$. Adapting the expression obtained for fully-depleted SOI films with inverted back surface [14], this definition gives:

$$V_{th,SOI} = 2\phi_F + V_{FB} + \frac{Q_D/2}{C_{ox}} \qquad (2\text{-}14)$$

where the depletion charge appears divided by 2 due to the charge sharing between identical front and back gates. This expression cannot be physically justified in double-gate structures where ϕ_S is not necessarily equal to $2\phi_F$ at threshold (as shown in Figures 2.2 and 2.4). Therefore the value given by (2-14) should not correspond to any experimental extraction method and the necessity arises to develop a threshold voltage definition that is directly based on the I_D-V_G curve.

The maximum transconductance change (TC) method [15], also called double derivative method, defines the threshold voltage as the gate voltage yielding the maximum value of $\partial^2 I_D / \partial V_G^2$. This method will be largely adopted throughout the text to extract V_{th} as a function of temperature and irradiation. It has been shown on various structures, that the TC method is able to extract multiple threshold voltages, each threshold corresponding to a different peak in the $\partial^2 I_D / \partial V_G^2$ -curve and to a different current onset [16]. This experimental method, very powerful owing to its simplicity, is therefore particularly well suited to provide both main and edge conduction thresholds often observed in n-channel GAA devices. Moreover, the TC method has been shown to be only slightly dependent on source and drain series resistances [15,17], because it makes use of the low drain current region where the channel resistance is high.

According to (2-11) and (2-4), V_{th} is the gate voltage such that:

$$\frac{d^3 I_D}{dV_G^3} = \frac{d^3 E_S}{dV_G^3} = \frac{d^3 \phi_S}{dV_G^3} = 0$$

Using the successive derivatives of (2-8) and (2-13), it emerges respectively:

$$V_{th,MIS} = 2\phi_F + V_{FB} + \frac{Q_D/2}{C_{ox}} + \frac{kT}{q}\left[\frac{1}{2} + \ln\left[\frac{C_{ox}}{4C_{si}}\left(1 + \frac{kT}{q}\frac{C_{ox}}{Q_D}\right)\right]\right] \quad (2\text{-}15)$$

and

$$V_{th,BL} = 2\phi_F + V_{FB} + \frac{Q_D/2}{C_{ox}}\sqrt{1 + \frac{kT}{q}\frac{C_{ox}}{Q_D/2}} + \frac{kT}{q}\ln\left(\frac{\frac{C_{ox}}{4C_{si}}}{1 - e^{-\frac{q}{kT}\frac{Q_D}{8C_{si}}}}\right) \quad (2\text{-}16)$$

The detailed calculations are provided in the Annex and are based on the following assumptions:

$$\frac{Q_D}{2} >> \frac{kT}{q}C_{ox} \text{ and } \frac{Q_D}{2} >> 4\frac{kT}{q}C_{si} \quad (2\text{-}17)$$

These conditions are verified in situations where the film doping concentration is high and/or the silicon film thickness is not too small, so that, at threshold, the depletion charge Q_D is not negligible compared to the inversion charge. Such situations, occurring with N^+ poly gate devices, exactly correspond to the region of validity already mentioned for the expression (2-13). Further using approximations (2-17), a common expression of the threshold voltage arises from (2-15) and (2-16):

$$V_{th,common} \approx 2\phi_F + V_{FB} + \frac{Q_D/2}{C_{ox}} + \frac{kT}{q}\left[\frac{1}{2} + \ln\left(\frac{C_{ox}}{4C_{si}}\right)\right] \quad (2\text{-}18)$$

Figure 2.8 confronts the BL approximation (2-16) (plain lines) and Medici simulations (dots) as a function of t_{si} in various conditions. Curves a, b and c, are obtained with N_A = 10^{17}, 10^{16} and $10^{15}cm^{-3}$ respectively. It should be mentioned that V_{FB} = -1V for curves a and b (N^+ poly gate devices) while curve c is computed with V_{FB} = 0.29V (P^+ poly gate devices). The latter curve is therefore shifted upward by about the bandgap voltage compared to curves a and b. Curves a, d and e show the influence of varying t_{ox} with $N_A = 10^{17}cm^{-3}$. Clearly, the model is robust against all parameter variations. Finally, Figure 2.8 also compares $V_{th,BL}$, $V_{th,MIS}$, $V_{th,SOI}$ and $V_{th,common}$ in the case of a light doping concentration (curve c).

- With quite large t_{si} and $N_A = 10^{17}cm^{-3}$ (curves a, d, and e with large t_{si} values), the variation of the threshold voltage with respect to process parameters is mainly due, as in regular SOI, to the depletion charge controlled by the gate, $qN_A t_{ox} t_{si}/2\varepsilon_{ox}$. V_{th} varies almost linearly with respect to t_{si}, t_{ox} and N_A and the sensitivity to one of these parameters decreases when the other parameters are reduced. Though not shown in Figure 2.8, $V_{th,MIS}$ and $V_{th,BL}$ give identical results. The classical expression $V_{th,SOI}$, as well as the simplified form $V_{th,common}$, although less accurate, are also relatively close to simulations.

- When t_{si} and/or N_A decreases (curves b and c for decreasing N_A; all curves when t_{si} drops), simplified forms (2-14) and (2-18) become totally inadequate. This means that

the correcting terms provided by $V_{th,MIS}$ and $V_{th,BL}$ play a more important part. Nevertheless, since assumptions (2-17) are less verified as well, the accuracy of $V_{th,MIS}$ and $V_{th,BL}$ is also expected to decrease. This is clearly observed for $V_{th,MIS}$ (curve c). On the other hand, $V_{th,BL}$ continues to correctly follow simulations.

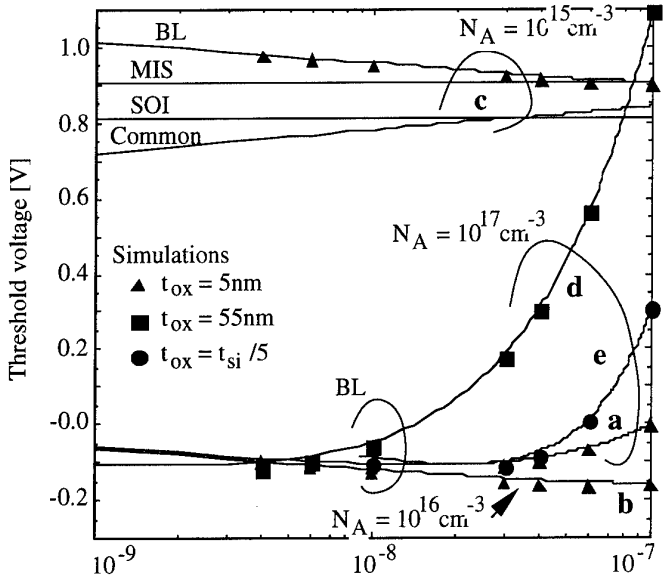

Figure 2.8: Threshold voltage as a function of silicon film thickness for analytical models and simulations (dots): a) t_{ox} = 5nm - $N_A = 10^{17}cm^{-3}$ - V_{FB} = -1V, b) t_{ox} = 5nm - $N_A = 10^{16}cm^{-3}$ - V_{FB} = -1V, c) t_{ox} = 5nm - $N_A = 10^{15}cm^{-3}$ - V_{FB} = 0.29V, d) t_{ox} = 55nm - $N_A = 10^{17}cm^{-3}$ - V_{FB} = -1V and e) $t_{ox} = t_{si}/5$ - $N_A = 10^{17}cm^{-3}$ - V_{FB} = -1V.

This surprising excellent agreement between BL model and simulations is highlighted in Figure 2.9 where the error $\varepsilon = V_{th,BL} - V_{th,Medici}$ is plotted against t_{si}.

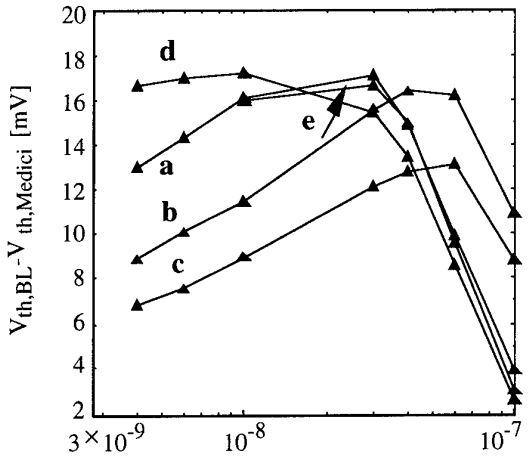

Figure 2.9: Absolute error of the threshold voltage given by the BL approximation when compared to Medici simulations as a function of the silicon film thickness: a) t_{ox} = 5nm - $N_A = 10^{17}cm^{-3}$ - V_{FB} = -1V, b) t_{ox} = 5nm - $N_A = 10^{16}cm^{-3}$ - V_{FB} = -1V, c) t_{ox} = 5nm - $N_A = 10^{15}cm^{-3}$ - V_{FB} = 0.29V, d) t_{ox} = 55nm - $N_A = 10^{17}cm^{-3}$ - V_{FB} = -1V and e) $t_{ox} = t_{si}/5$ - $N_A = 10^{17}cm^{-3}$ - V_{FB} = -1V.

$V_{th,Medici}$ is obtained with an accuracy of ±5mV. Since assumptions (2-17) suffer from the decrease of t_{si}, the error ε raises steadily from t_{si} = 100nm down to the range 30...10nm. However, as soon as t_{si} < 10nm, the accuracy suddenly raises again and ε never exceeds 0.02V although the different parameters vary by orders of magnitude! It should be noted that, with t_{si} below 10nm, quantum mechanics should be used so that the results presented here must be interpreted with the greatest care and need to be confirmed.

The Annex shows that the correcting terms added in the expression of $V_{th,BL}$ to the simple formulation $V_{th,SOI}$ modifies both the surface electric field and the surface potential at threshold:

$$E_S^* = \frac{Q_D/2}{\varepsilon_{si}}\sqrt{1+\frac{kT}{q}\frac{C_{ox}}{Q_D/2}}$$

$$\phi_S^* = 2\phi_F + \frac{kT}{q}\ln\left(\frac{\frac{C_{ox}}{4C_{si}}}{1-e^{-\frac{q}{kT}\frac{Q_D}{8C_{si}}}}\right) \qquad (2\text{-}19)$$

• The first term of E_S^* results from the depletion charge controlled by each of the gates. The additional contribution is due to presence of the inversion charge and increases with decreasing N_A, t_{si} and t_{ox}, conditions in which the inversion charge grows compared to the depletion charge.

• As far as the surface potential is concerned, the thinner the silicon film, the lower the surface potential at threshold (at fixed gate oxide thickness and assuming a negligible influence of the exponential term in (2-19)). ϕ_S^* becomes lower than the $2\phi_F$ strong inversion limit as soon as $t_{si} < 4t_{ox}\varepsilon_{si}/\varepsilon_{ox} \approx 12t_{ox}$, and this is usually verified. For N^+ poly gate devices (corresponding to Figure 2.2), $t_{si} = 1.36t_{ox}$ and $\phi_S^* = 0.753V < 2\phi_F = 0.815V$, which justifies the concern about weak inversion mechanisms. Also, when the device is scaled at constant ratio t_{si}/t_{ox}, the surface potential at threshold should be unchanged (when N_A is sufficiently large).

Finally, the very small dependence of V_{th} on t_{si} presented by curves b-c (in comparison to curves a-d-e) in Figure 2.8, is generally the major argument to recommend the use of a lightly-doped channel region. However, with N^+ poly gates (curve b), V_{th} is negative. On the other hand, with P^+ poly gates (curve c), V_{th} is too large for low voltage applications. Therefore, Suzuki *et al.* [18,19,20,21] suggest to use N^+ back gates and P^+ front gates. In this case, the resulting threshold voltage adopts a kind of mean value and, with N_A as small as $10^{15}cm^{-3}$, V_{th} is in the range 0.0...0.5V. Advanced technologies also introduce tantalum as midgap gate material [22].

4. Current improvement in double-gate devices

Two years before the first double-gate devices were realized, Cristoloveanu *et al.* already proposed the concept of volume inversion [23]. They suggest that when the carriers are no more confined at an interface but are rather spread out in the silicon

volume, higher current and transconductance should be observed, as a result of larger number of minority carriers, reduced influence of surface scattering due to lower perpendicular electric field, and enhanced volume mobility. The first experimental confirmations have been obtained connecting back and front gates in regular SOI devices. Later on, 2.5 to 3 times drain current enhancements were reported from threshold to strong inversion regions in real double-gate devices [24,25].

However, Venkatesan *et al.* [3] pointed out that, single and double-gate devices being measured at same gate voltage, such improvements could be partially influenced by inherent additional current due to the lowered threshold voltage of double-gate devices. Furthermore, the devices which are compared generally do not have exactly the same width nor the same doping level. Following Reference [3], no current improvement should be observed when single and double-gate devices are compared at same gate voltage overdrive in the strong inversion regime, which is the practically useful region of operation. This debate is still open as shown by the recent correspondence [26].

Our own experience tends to indicate that single and double-gate devices, having exactly the same width and same doping concentration (same wafer), show a small improvement of transconductance over the expected factor of 2, even when compared at same gate voltage overdrive. This enhancement is nevertheless only appreciable in the threshold region, and rapidly vanishes in the strong inversion region (Figure 1.10). Analytical models enable us to put some light into the controversy. The part of the enhancement imputable to the number of available carriers $Q_N = \int qn(x)dx$ and to the larger volume mobility will be discussed. Furthermore, the impact of the gate bias will be clarified.

At large t_{si}, the two interfaces of double-gate devices do not interact and just twice the carrier concentration of single-gate devices (with infinitely thick buried oxide layer or equivalent back-gate bias condition) should be obtained. As suggested in [13], shrinking t_{si} with t_{ox} and N_A both constant, reveals the influence of the double-gate structure on the carrier spreading. Figure 2.10 plots the normalized total number of carriers $Q_N(t_{si})/Q_N(100nm)$ as a function of t_{si}. The gate oxide thickness is fixed at 5nm, the minimum value practical for reliability concerns, and a low doped film is considered ($N_A = 1.5\times10^{15}cm^{-3}$). Dots are provided from Medici simulations. Smooth lines are obtained with the MIS model (2-8) and (2-11) whose accuracy has been proved to be nearly independent on the potential shape. Two different gate bias conditions are investigated:

- constant gate voltage (open dots, dashed lines): from A to B, V_G is swept from V_{th0}-0.2V to V_{th0}+0.6V by steps of 0.2V [13] where V_{th0} is the threshold voltage obtained by simulations for t_{si} = 100nm.
- constant gate voltage overdrive (black dots, plain lines): from A to B, V_G-V_{th} is swept from -0.2V to 0.6V by steps of 0.2V with V_{th} given by the BL approximation (2-16). The BL model has been chosen because it ensures a correct evolution of V_{th} throughout the full range of t_{si} variation (Figure 2.9).

Correct agreement between model and simulations is again observed.

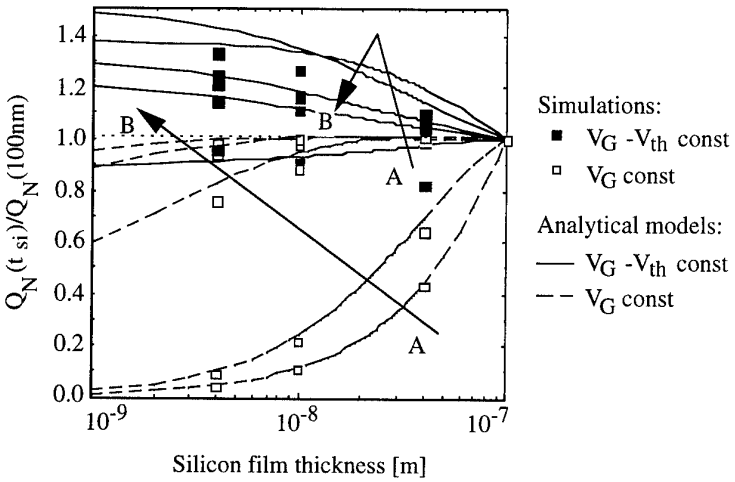

Figure 2.10: Normalized free charge $Q_N(t_{si})/Q_N(100nm)$ as a function of the silicon film thickness at constant gate voltage and constant gate voltage overdrive: $N_A = 1.5\times10^{15}cm^{-3}$, $t_{ox} = 5nm$.

To further assist the discussion, Figure 2.11 presents $Q_N(10nm)/Q_N(100nm)$ as a function of V_G-V_{th0} (circles) or V_G-V_{th} (squares) for lightly doped films (open symbols) and heavily doped films (dark symbols). Those results were obtained by simulations.

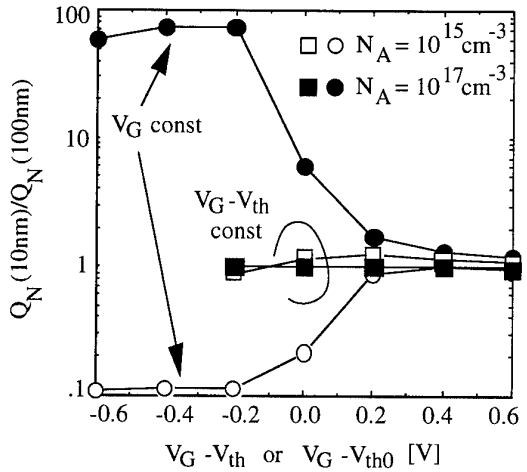

Figure 2.11: Simulated normalized free charge $Q_N(10nm)/Q_N(100nm)$ as a function of V_G-V_{th0} (constant gate voltage) or V_G-V_{th} (constant gate voltage overdrive) for $N_A = 1.5\times10^{15}cm^{-3}$ and $N_A = 10^{17}cm^{-3}$, $t_{ox} = 5nm$.

As clearly shown in Figures 2.10 and 2.11, $Q_N(t_{si})/Q_N(100nm)$ is strongly above (below) unity when working at constant gate voltage in heavily(lightly) doped films. In HD films, as suspected by Venkatesan *et al.*, a current improvement is inherent to the strong drop of the threshold voltage with reduced t_{si} as plotted in Figure 2.8 (curve a). $Q_N(t_{si})/Q_N(100nm)$ reaches 10 to 100 in the sub- and near-threshold regions and rapidly drops down to the 1.1...1.5 range in the strong inversion region. It is therefore difficult to estimate the additional benefit of larger volume mobility, at least in the (sub)threshold region. The reverse situation arises in LD films, with Q_N dropping linearly with t_{si} below threshold and remaining just below unity well above threshold. The explanation is simple: in the subthreshold region, the potential of LD films is very flat as previously discussed

in relation to Figure 2.4, and hence correctly approximated by the MIC0 model. Combining of (2-5) and (2-11), it comes:

$$E_S = \frac{q(N_A + n_0)}{\varepsilon_{si}} \frac{t_{si}}{2} \qquad \text{and} \qquad Q_N = qn_0 t_{si} \tag{2-20}$$

At constant V_G, ϕ_S, and hence $n_0 \approx n_S$, are approximately constant since the threshold voltage is nearly insensitive to t_{si} (Figure 2.8, curve c). Hence Q_N shrinks with t_{si} so that less carriers are available. The current improvement brought by wider carrier spreading could hence be masked, the decrease of n(x) compensating the increase of $\mu(x)$. Comparing single- and double-gate devices at same gate voltage is hence definitively not a good solution to detect the influence of larger volume mobility.

Now, working at same gate voltage overdrive, Figures 2.10 and 2.11 show that an enhancement of Q_N by a factor 1.1...1.2 exists around threshold when t_{si} is decreased down to a few tens of nanometers. This enhancement is smaller in HD films, slightly larger when t_{si} < 10nm, and rapidly vanishes above threshold. In agreement with Cristoloveanu *et al.*, a slightly larger number of minority carriers could hence be partially responsible for current enhancements observed experimentally in double-gate devices compared to their single-gate counterparts at same gate voltage overdrive, at least in the threshold region.

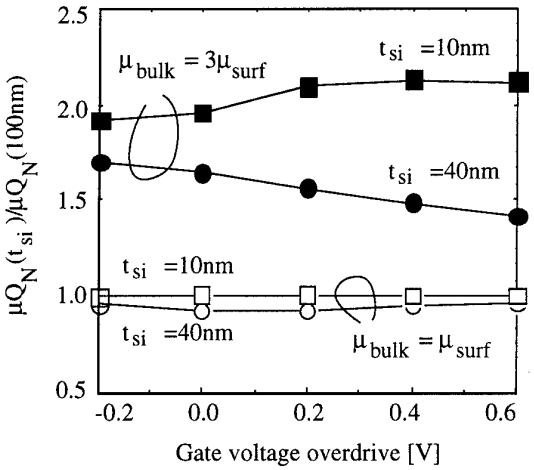

Figure 2.12: Simulated normalized integral $\mu Q_N(t_{si})/\mu Q_N(100nm)$ as a function of the gate voltage overdrive with t_{si} as parameter, when the bulk mobility equals the surface mobility or is three times higher. $N_A = 10^{17}cm^{-3}$ and t_{ox} = 5nm.

Figure 2.12 shows the normalized integral $\mu Q_N(t_{si})/\mu Q_N(100nm)$ as a function of gate voltage overdrive in a heavily doped film with t_{si} as parameter. The integral is defined as $\mu Q_N(t_{si}) = \int_0^{t_{si}} n(x)\mu(x)dx$ with n(x) obtained from simulations. The mobility profile is step-like with the volume mobility μ_{bulk} three times higher than the surface mobility μ_{surf}. This assumption is in accordance with mobility profiles deduced from transport measurements in SOI devices [23] where $\mu_n = 1200cm^2/Vs$ in the center of the film, $500cm^2/Vs$ at the front interface, and $400cm^2/Vs$ at the back interface. Results with $\mu_{bulk} = \mu_{surf}$ are shown in Figure 2.12 as well, for comparison. The depth of the inversion layer affected by surface mobility is assumed to be $t_{si}/20$. Figure 2.12 indicates that,

owing to larger volume mobility, the maximum current enhancement is in the range 1.5 to 2 and could appear above threshold. When combined to the factor 2 coming from double-gate conduction, a factor of 3 or more appears, which qualitatively matches previously reported measurements as well as results presented in Figure 1.10. However, we would warn the reader that these deductions are strongly sensitive to our choice of the inversion layer depth. Also, results obtained for t_{si} = 10nm could be criticized because bulk and surface conduction should merge in such thin films. Furthermore, devices with different t_{si} are compared at same gate voltage overdrive with the threshold voltage extracted by the TC method from Q_N-V_G curves. Considering another extraction method or μQ_N-V_G curves could change predictions of Figure 2.12.

In general, at same t_{si} and t_{ox}, lowering N_A results in a flatter potential shape, even above threshold, which should provide better volume inversion. With $N_A = 10^{15}cm^{-3}$, $\mu Q_N(t_{si})/\mu Q_N(100nm)$ is slightly smaller than obtained with $N_A = 10^{17}cm^{-3}$, which tends to prove that the potential is already so flat for t_{si} = 100nm that the volume mobility enhancement is less visible when t_{si} shrinks. Obtaining useful devices with low N_A can be achieved at the expense of proper gate work function engineering as already explained (P^+ gates, P^+ front/N^+ back gates, tantalum gates, ...).

The previous study just gives an insight into the contributions of volume mobility and larger number of minority carriers to the current improvements observed experimentally in double-gate devices. The essential conclusion is that results are very hard to interpret with certitude. The gate bias adequate to perform the comparison of single- and double-gate devices is around the threshold voltage but is not clearly defined and certainly strongly influences of the results.

5. Transconductance

The transconductance g_m corresponding to the current in linear operation (2-11) is:

$$g_m = \frac{\partial I_D}{\partial V_G} = 2\mu_n C_{ox} \frac{W}{L}\left[\frac{\varepsilon_{si}}{C_{ox}}\frac{\partial E_S}{\partial V_G}\right] \tag{2-21}$$

with dE_S/dV_G extracted from relationship (2-8) (MIS model) or (2-13) (BL model). The factor 2 still originates from front and back gate conduction. After straightforward manipulations, the final expressions of the transconductance are:

$$g_{m,MIS} = 2\frac{W}{L}C_{ox}\mu_n V_{DS}\frac{\dfrac{q}{C_{ox}}\dfrac{n_S}{E_S}}{\dfrac{1-\dfrac{q}{2C_{si}}\dfrac{n_S}{E_S}e^{-\frac{q}{kT}\frac{t_{si}}{2}E_S}}{1-e^{-\frac{q}{kT}\frac{t_{si}}{2}E_S}}+\dfrac{q}{C_{ox}}\dfrac{n_S}{E_S}+\dfrac{q}{\varepsilon_{si}}\dfrac{kT}{q}\dfrac{n_S}{E_S^2}} \tag{2-22}$$

$$g_{m,BL} = 2\frac{W}{L}C_{ox}\mu_n V_{DS}\frac{\frac{q}{C_{ox}}\frac{n_S}{E_S}\left(1-e^{\frac{-q}{kT}\frac{Q_D}{8C_{si}}}\right)}{1+\frac{q}{C_{ox}}\frac{n_S}{E_S}\left(1-e^{\frac{-q}{kT}\frac{Q_D}{8C_{si}}}\right)} \quad (2\text{-}23)$$

from (2-8) and (2-13), respectively. A common simplified form of g_m is obtained using approximations (2-17) previously introduced to simplify the threshold voltage expression:

$$g_{m,common} \approx 2\frac{W}{L}C_{ox}\mu_n V_{DS}\frac{\frac{q}{C_{ox}}\frac{n_S}{E_S}}{1+\frac{q}{C_{ox}}\frac{n_S}{E_S}} \quad (2\text{-}24)$$

Figure 2.13 compares the normalized transconductance $g_{m,MIS}/(\mu_n V_{DS}W/L)$ to Medici simulations in a wide variety of conditions combining two doping concentrations ($N_A = 10^{17}$ and $10^{15}cm^{-3}$) and two film thicknesses (t_{si} = 100 and 10nm). The accuracy of the MIS model is excellent in all conditions. As already discussed for the current, the model is just slightly less precise in a short portion of the gate voltage range situated above threshold. Again, we have verified that expression (2-23), coming from the BL model, provides a greater accuracy than the MIS model when the doping concentration and the film thickness are large ($N_A = 10^{17}cm^{-3}$ and t_{si} > 50nm). However, $g_{m,BL}$ should be strictly dedicated to those situations since it yields significantly worst results when either N_A or t_{si} decreases. The same observations are valid for the common expression (2-24). The normalized transconductance presented in Figure 2.13 does not include the mobility and is hence free of degradations linked to perpendicular surface electric field, carrier concentration and source/drain resistances. As a result, the normalized g_m increases monotonously with V_G and tends to $2C_{ox}$. Such degradations should be accounted for to reproduce experimental data presented in Figure 1.11, and will be discussed in Chapter III.

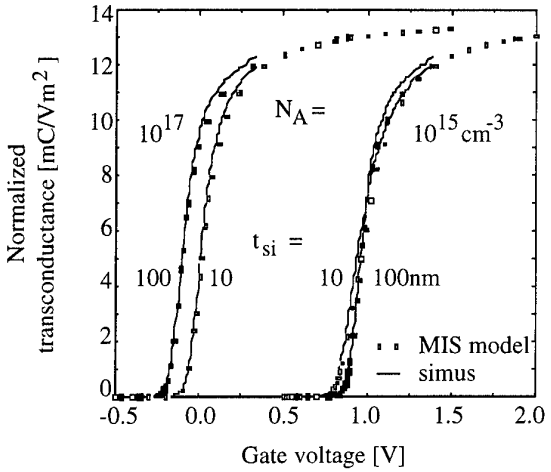

Figure 2.13: Normalized transconductance $g_{m,MIS}/(\mu_n V_{DS}W/L)$ as a function of gate voltage obtained by the MIS model and by simulations with t_{ox} = 5nm.

We will now assume that the transconductance is a measure of how fast the surface potential (and hence the surface electron concentration) reacts to an increase of the gate voltage or, equivalently, to an increase of the charge stored in the film: $g_m \div (\Delta n_S / \Delta Q_N)$. When the potential distribution is very flat, $\Delta Q_N \approx t_{si} \Delta n_S$. Hence, the thinner the film, the larger g_m should be. This can be verified in Figure 2.13 where the g_m-curve raises sharply when t_{si} decreases in case of low doping. Even more clear, is Figure 2.14, presenting the normalized g_m extracted from simulations as a function of t_{si} at $V_G = V_{th}$ and $V_G = V_{th}+0.2V$. The increase of g_m with reduced t_{si} strengthens when t_{si} or N_A are very small, conditions in which the potential distribution is indeed very flat. On the other extreme, assuming a bulk-like potential bending, the inversion charge is approximately spread out over the distance corresponding to a potential drop by kT/q [27]: $\Delta Q_N \approx \Delta n_S \, kT/(qE_S)$. In this case, the higher the doping concentration, the larger the transconductance should be, since E_S increases with N_A. This prediction is again verified in Figure 2.14, at least at large t_{si}, which precisely corresponds to large potential bendings.

g_m varies however very few when parameters are swept so that the enhancement of the transconductance by more than a factor 2, reported in Chapter I between GAA and SOI devices, should be interpreted in terms of higher volume mobility only.

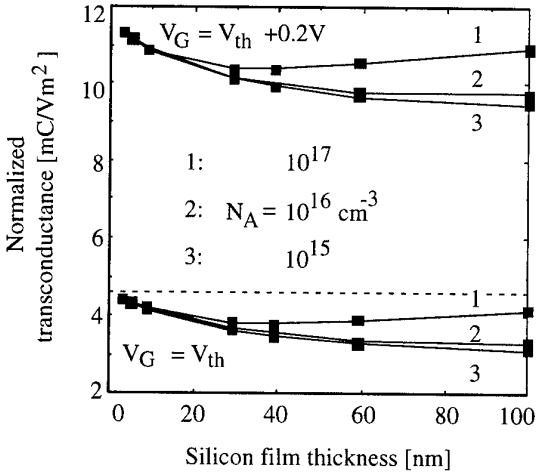

Figure 2.14: Normalized transconductance $g_m/(\mu_n V_{DS} W/L)$ extracted from simulations at $V_G = V_{th}$ and $V_G = V_{th}+0.2V$ with t_{ox} = 5nm, as a function of the silicon film thickness.

Finally, the Annex shows how, starting from (2-19), it comes $n_S^*/E_S^* \approx C_{ox}/2q$ at threshold. Inserting this result in the expression of $g_{m,common}$, the normalized transconductance at threshold becomes $g_m^*/(\mu_n V_{DS} W/L) \approx 2C_{ox}/3$, level indicated by the dashed line in Figure 2.14. This good guess of exact simulation results has already been reported for regular SOI devices (the factor 2 being dropped).

6. Subthreshold region

6.1. Subthreshold current

From (2-11) and (2-13), the inversion charge can be written as:

$$Q_N = Q_D\left[\sqrt{1+\frac{8C_{si}}{Q_D}\frac{kT}{q}\left[1-e^{\frac{-q}{kT}\frac{Q_D}{8C_{si}}}\right]e^{\frac{q}{kT}(\phi_S-2\phi_F)}}-1\right]$$

In the subthreshold region, additional simplifying assumptions allow to reach an explicit expression of the current. First of all, below threshold, the exponential term including ϕ_S is negligible compared to unity so that the linear approximation of the square root is valid:

$$Q_N = 4C_{si}\frac{kT}{q}\left[1-e^{\frac{-q}{kT}\frac{Q_D}{8C_{si}}}\right]e^{\frac{q}{kT}(\phi_S-2\phi_F)}$$

Furthermore, E_S may be replaced by its value coming from the depletion approximation (2-1). Using Gauss' law (2-4), Q_N becomes:

$$Q_N(y) = 4C_{si}\frac{kT}{q}\left[1-e^{\frac{-q}{kT}\frac{Q_D}{8C_{si}}}\right]e^{\frac{q}{kT}\left(V_G-V_{FB}-\frac{Q_D/2}{C_{ox}}-2\phi_F-V(y)\right)} \qquad (2\text{-}25)$$

where the dependence on the voltage applied between source and drain V(y) has been introduced. Still assuming a constant mobility profile and integrating from source to drain, we obtain an explicit expression of the I_D-V_G characteristic:

$$\begin{aligned} I_D &= \frac{W}{L}\mu_n\int_0^{V_D}Q_N(y)dy \\ &= \frac{W}{L}\mu_n 4C_{si}\left(\frac{kT}{q}\right)^2\left[1-e^{\frac{-q}{kT}\frac{Q_D}{8C_{si}}}\right]e^{\frac{q}{kT}\left(V_G-V_{FB}-\frac{Q_D/2}{C_{ox}}-2\phi_F\right)}\left[1-e^{\frac{-q}{kT}V_D}\right] \end{aligned} \qquad (2\text{-}26)$$

This expression can be compared to the result yielded by the classical bulk analysis [27] where the diffusion subthreshold current is given by:

$$\begin{aligned} I_D &= qA\mu_n\frac{kT}{q}\frac{n(0)-n(L)}{L} \\ &= q\frac{2Wt_x}{L}\mu_n\frac{kT}{q}N_A e^{\frac{q}{kT}(\phi_S-2\phi_F)}\left[1-e^{-\frac{q}{kT}V_D}\right] \end{aligned}$$

A is the cross-section of the current flow, and n(0) and n(L) are the electron densities in the channel at source and drain respectively. The area of the current flow is approximated by $2Wt_x$, where t_x is the effective channel thickness corresponding to the distance where the potential decreases by kT/q (which gives $n_S/n_x = 2.718$). At first order approximation, t_x is hence equal to $kT/(qE_S)$. Finally, using the depletion approximation (2-1) for the surface electric field and Gauss' law (2-4), it comes:

$$I_D = \frac{W}{L}\mu_n\left(\frac{kT}{q}\right)^2 4C_{si}e^{\frac{q}{kT}\left(V_G - V_{FB} - \frac{Q_D/2}{C_{ox}} - 2\phi_F\right)}\left[1 - e^{-\frac{q}{kT}V_D}\right] \qquad (2\text{-}27)$$

which differs from (2-25) by the term $\kappa = \left[1 - e^{\frac{-q}{kT}\frac{Q_D}{8C_{si}}}\right]$.

Figure 2.15 compares, to Medici simulations, the mobile charge Q_N, calculated with (curves 1 to 5) and without (curves 1' to 5') the term κ, when t_{si}, t_{ox} and N_A are varied by orders of magnitude. It appears that κ improves significantly the accuracy of the model (2-25, 2-26) compared to the classical formulation (2-27) as soon as t_{si} and/or N_A decreases. Indeed, with t_{si} = 100nm and $N_A = 10^{17}cm^{-3}$ curves 2-2' and 3-3', obtained respectively with t_{ox} = 5 and 55nm, are nearly the same. However, curves 1-1' and 5-5', obtained respectively with reduced N_A and t_{si}, split apart. The improvement provided by κ is especially remarkable when looking at curves 4-4' where both t_{si} and N_A are reduced.

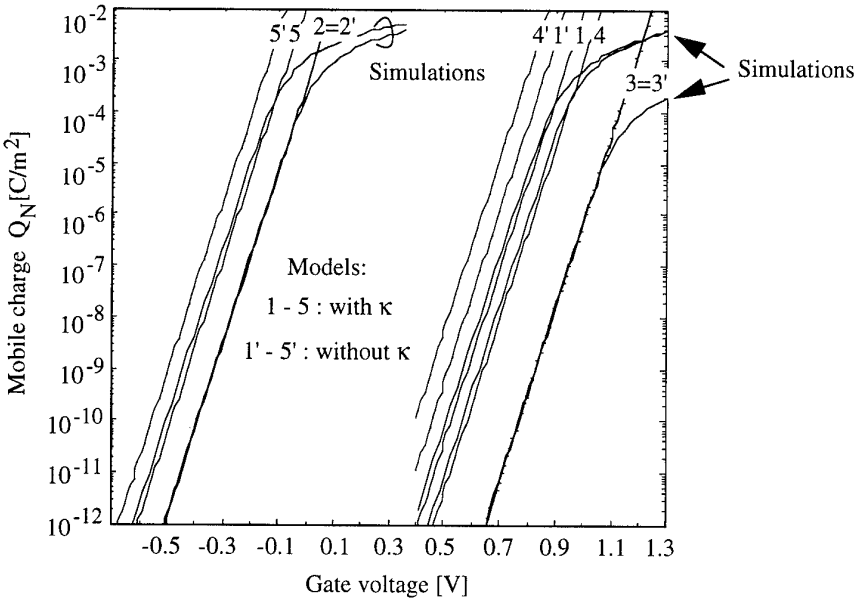

Figure 2.15: Improved (with κ) and classical (without κ) subthreshold free charge as a function of the gate voltage with t_{si}, t_{ox} and N_A as parameters: t_{si}[nm] - t_{ox}[nm] - N_A[cm^{-3}] = 1) 100 - 5 - 10^{15} ; 2) 100 - 5 - 10^{17} ; 3) 100 - 55 - 10^{17} ; 4) 10 - 5 - 10^{15} ; 5) 10 - 5 - 10^{17}.

6.2. Subthreshold slope

The inverse subthreshold slope is defined as $S = \left[\partial \log_{10}(I_D)/\partial V_G\right]^{-1}$. From (2-26) and (2-27), S reaches the ideal value $\ln(10)(kT/q) = 0.059533\,V/dec$ which is the best figure that can be achieved in MOSFETs. As already demonstrated by Wouters *et al.* [28], the symmetrical control of the gate on the body potential by both sides of the thin film induces a perfect capacitive coupling between V_G and ϕ_S, as sketched in Figure 2.16a.

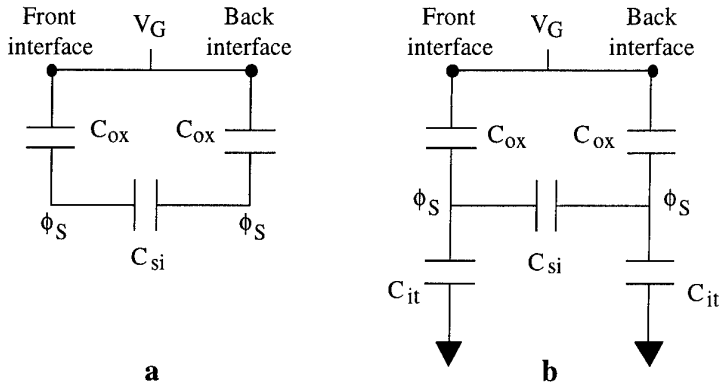

Figure 2.16: Equivalent capacitor network for a double-gate device from [28]: a) without interface traps; b) with an interface trap density D_{it}.

As a result, below threshold, both surface and body potentials linearly follow the gate bias as shown in Figures 2.2 and 2.4. S-values provided by simulations do not differ from the ideal analytical prediction as shown in Figure 2.17 where S only slightly degrades at increasing t_{ox} and is virtually independent on t_{si} and N_A.

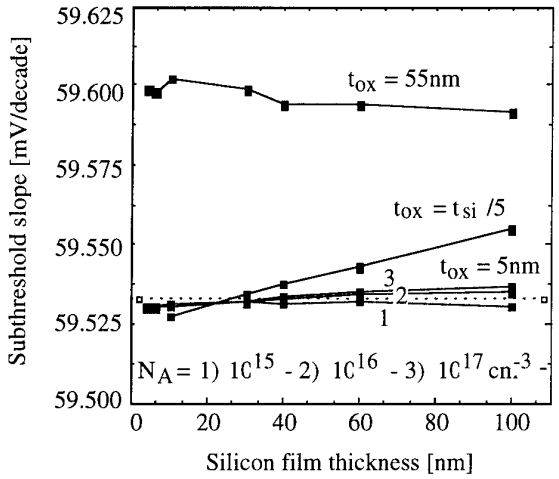

Figure 2.17: Simulated subthreshold slope as a function of the silicon film thickness with the gate oxide thickness and the doping concentration as parameters.

When a uniform density of interface traps D_{it} exists in the bandgap, Gauss' Law becomes:

$$\frac{\varepsilon_{si}}{C_{ox}} E_S = V_G - V_{FB} - \phi_S \left(1 + \frac{qD_{it}}{C_{ox}}\right)$$

and the subthreshold slope is:

$$S = \ln(10)\frac{kT}{q}\left[1+\frac{C_{it}}{C_{ox}}\right] \qquad (2\text{-}28)$$

with $C_{it} = qD_{it}$. The equivalent capacitive scheme is depicted in Figure 2.16b. The values obtained experimentally in Chapter I (S_n = 0.062V/dec and S_p = 0.064V/dec) correspond to an interface trap density D_{it} equal to $2.94\times10^{10}cm^{-2}eV^{-1}$ and $1.62\times10^{10}cm^{-2}eV^{-1}$ in n- and p-channel devices, respectively. These are typical values of good quality gate oxides.

7. Conclusions

One-dimensional analytical models for the current, the transconductance, the threshold voltage and the subthreshold slope were developed and discussed for nMOS ultra-thin double-gate devices. Their common starting point is that both the doping impurity charges and the electron concentration should be simultaneously considered to obtain expressions continuously valid from subthreshold to strong inversion regions.

Two models are especially relevant.

• The first approach provides a potential distribution across the film which is very accurate when the film doping concentration is high (such as in devices made with N^+ poly gates). When N_A or t_{si} decreases, relevant values of ϕ_S, E_S, I_D and g_m are still obtained although the mid-film potential becomes strongly overestimated. The major quality of this model is its versatility: it provides correct accuracy for the current independently of the set of process parameters and the operating conditions.

• Another model skips one integration of Poisson's equation and therefore gives surface parameters but not the full potential distribution. This model is very sensitive to the choice of the process parameters. Starting with a very poor accuracy, it becomes more and more reliable when both N_A and t_{si} increase and, ultimately, this model becomes more efficient than the first approximation. Its huge advantage is that it provides a very robust expression of the threshold voltage curiously valid when both N_A and t_{si} vary over two orders of magnitude.

Combining these two approaches, a complete set of expressions is available for I_D, g_m and V_{th}. Although restricted to long-channel devices in linear operation, this study significantly outperforms previous works in terms of physical insight on the volume inversion mechanisms.

• When the depletion charge is large (high N_A), the potential bending, already important in the subthreshold region, only slightly varies with gate voltage. As a result, a nearly constant (and relatively small) fraction of the silicon film participates to the current conduction. Also, a large portion of the film stays below the $2\phi_F$ limit of strong inversion onset and the surface potential at threshold, extracted by the TC method, is found below $2\phi_F$, confirming the occurrence of the current following a

weak inversion mechanism. Classical models fail and both new approaches are especially accurate and useful in a wide portion of the gate voltage range around threshold where neither the fixed charges nor the mobile charges are negligible.

• On the contrary, when N_A is low, the device suddenly switches from the depletion region where the potential is nearly rigorously flat and volume conduction is evident, to the strong inversion operation, where charges are located below the surface. The first model correctly represents both regions and its continuity is highly appreciated. The second model produces a correct expression of V_{th}. In strong inversion, the volume contribution to the global conduction is marginal even if the whole potential distribution exceeds $2\phi_F$.

This physical interpretation of volume conduction allows to clarify the debate about the improvement of current and transconductance by more than a factor of 2 over conventional SOI devices: when devices are compared at same gate voltage overdrive, a significant enhancement should only be observed due to higher volume mobility, below and around threshold, especially in lightly doped films.

Finally, the subthreshold slope is ideal owing to the perfect control of the surrounding gate on the body potential, and could only be degraded by the presence of interface states.

We will now examine the GAA device characteristics in various harsh contexts such as high temperature ambiance, large power operation and radiative environments.

Annex

The TC method defines the threshold voltage as the gate voltage giving:

$$\frac{d^3 I_D}{dV_G^3} = \frac{d^3 E_S}{dV_G^3} = \frac{d^3 \phi_S}{dV_G^3} = 0 \tag{A-1}$$

We have shown in the text that, solving Poisson's equation with two different approximations (BL and MIS), the surface electric field can be obtained from two distinct implicit equations ((2-13) and (2-8)), rewritten here for clarity:

$$E_S(y) = \sqrt{\frac{2qN_A}{\varepsilon_{si}}} \cdot \sqrt{\frac{Q_D}{8C_{si}} + \frac{kT}{q}\frac{n_i^2}{N_A^2} e^{\frac{q}{kT}\left[V_G - V_{FB} - \frac{\varepsilon_{si}}{C_{ox}} E_S\right]} \left(1 - e^{\frac{-q}{kT}\left[\frac{Q_D}{8C_{si}}\right]}\right)}} \tag{A-2}$$

$$E_S + \frac{kT}{q}\frac{qn_S}{\varepsilon_{si} E_S}\left(e^{-\frac{q}{kT}\frac{t_{si}}{2}E_S} - 1\right) - \frac{Q_D/2}{\varepsilon_{si}} = 0 \tag{A-3}$$

This Annex demonstrates that, using the following assumptions:

$$\frac{Q_D}{2} >> \frac{kT}{q} C_{ox} \text{ and } \frac{Q_D}{2} >> 2\frac{kT}{q}\left[C_{si} - \frac{C_{ox}}{4}\right]$$

these two equations provide explicit expressions of the threshold voltage.

• <u>From the BL model (A-2)</u>

Using Gauss' law (2-4), (A-2) is rewritten as:

$$V_G = \phi_S + V_{FB} + \frac{Q_D/2}{C_{ox}}\sqrt{1 + \frac{1}{\alpha}\frac{Q(\phi_S)}{Q_D}} \tag{A-4}$$

with

$$Q(\phi_S) = Q_D e^{\frac{q}{kT}(\phi_S - 2\phi_F)}\left(1 - e^{-\alpha}\right) \tag{A-5}$$

and

$$\alpha = \frac{q}{kT}\frac{Q_D}{8C_{si}}$$

$Q(\phi_S)$ is the charge controlled by the gate, arising from the contribution of the minority carrier concentration. It should be noted that $\alpha(kT/q)$ is, from (2-9), the difference

between surface and mid-film potential ϕ_S-ϕ_S below threshold. It will also be useful to define:

$$\delta = \frac{C_{ox}}{4C_{Si}}. \text{ We have also } \frac{\delta}{\alpha} = \frac{kT}{q}\frac{C_{ox}}{Q_D/2}$$

δ compares the silicon film to the gate oxide thickness. δ/α depends on all process parameters.

The successive differentials of (A-4) and (A-5) with respect to V_G yield:

$$\begin{aligned}
\frac{d\phi_S}{dV_G} &= \frac{1}{1+u} \\
\frac{d^2\phi_S}{dV_G^2} &= \frac{-q}{kT}\frac{u(1-v)}{(1+u)^3} \\
\frac{d^3\phi_S}{dV_G^3} &= -\left(\frac{q}{kT}\right)^2 \frac{u(1-2u-3v(1-u-v))}{(1+u)^5}
\end{aligned} \qquad \text{(A-6)}$$

with the following definitions:

$$u = u(\phi_S) = \frac{\alpha}{2\delta}\frac{\frac{1}{\alpha}\frac{Q(\phi_S)}{Q_D}}{\sqrt{1+\frac{1}{\alpha}\frac{Q(\phi_S)}{Q_D}}} \qquad v = v(\phi_S) = \frac{1}{2}\frac{\frac{1}{\alpha}\frac{Q(\phi_S)}{Q_D}}{\left(1+\frac{1}{\alpha}\frac{Q(\phi_S)}{Q_D}\right)}$$

Numerically solving (A-1) with (A-6), we obtain the contribution of minority carriers at threshold $Q(\phi_S^*)$, shown in Figure A.1 as a function of the ratio δ/α.

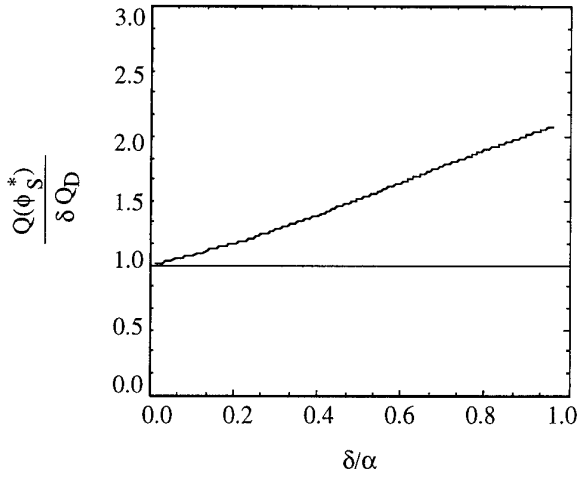

Figure A.1: Value of the ratio $Q(\phi_S^*)/\delta Q_D$ at threshold as a function of the parameter δ/α.

If the model is restricted to the region where $\delta/\alpha << 1$, we observe that $Q(\phi_S^*)$ can be approximated by:

$$Q(\phi_S^*) = \delta Q_D \qquad \text{(A-7)}$$

$\delta/\alpha << 1$ corresponds to $(Q_D/2) >> (kT/q)C_{ox}$ and is verified in situations where the film doping concentration is high. In this case, the depletion charge Q_D is not negligible compared to the inversion charge at threshold $Q(\phi_S^*)$. This exactly corresponds to the region of validity already mentioned for relationship (A-2).

From (A-7) and (A-5), the following surface potential at threshold is obtained:

$$\phi_S^* = 2\phi_F + \frac{kT}{q}\ln\left[\frac{\delta}{1-e^{-\alpha}}\right] \tag{A-8}$$

When N_A is high, $\alpha >> 1$ and the exponential term in (A-8) drops. The threshold voltage is finally obtained when combining (A-4) and (A-8):

$$V_{th} = 2\phi_F + V_{FB} + \frac{kT}{q}\left[\frac{\alpha}{\delta}\sqrt{1+\frac{\delta}{\alpha}} + \ln\left(\frac{\delta}{1-e^{-\alpha}}\right)\right] \tag{A-9}$$

$$V_{th} \approx 2\phi_F + V_{FB} + \frac{Q_D/2}{C_{ox}} + \frac{kT}{q}\left[\frac{1}{2} + \ln\left(\frac{C_{ox}}{4C_{si}}\right)\right] \tag{A-10}$$

At threshold, it is easy to verify that $\frac{n_S^*}{E_S^*} = \frac{C_{ox}}{2q}\frac{1}{\left(1-e^{-\alpha}\right)\sqrt{1+\frac{\delta}{\alpha}}} \approx \frac{C_{ox}}{2q}$ (A-11)

• <u>From the MIS model (A-3)</u>

When $t_{si}E_S >> 2(kT/q)$, (A-3) reduces to:

$$E_S - \frac{kT}{q}\frac{qn_S}{\varepsilon_{si}E_S} - \frac{Q_D/2}{\varepsilon_{si}} = 0$$

from which the successive derivatives of E_S with respect to V_G are extracted and finally (A-1) gives:

$$3\left(\frac{1}{\Delta E^2} + \frac{1}{E_S^{*2}}\right)^2 = \left[\frac{2}{\Delta E^3} + \frac{1}{\Delta E}\frac{1}{E_S^{*2}} + \frac{1}{\Delta E^2}\frac{1}{E_S^*} + \frac{1}{E_S^{*3}}\right]\left[\frac{1}{\Delta E} - \frac{1}{E_S^*} - \frac{q}{kT}\frac{\varepsilon_{si}}{C_{ox}}\right] \tag{A-12}$$

with

$$\Delta E = \frac{Q_D/2}{\varepsilon_{si}} - E_S^* = \frac{kT}{q}\frac{q}{\varepsilon_{si}}\frac{n_S^*}{E_S^*} \tag{A-13}$$

ΔE is the difference between the surface electric field coming from the depletion approximation (2-1) and the MIS model.

Assuming that $E_S^* >> \Delta E$ (the surface electric field is much larger than its correcting term), equation (A-12) yields $\Delta E = -(C_{ox}/2\varepsilon_{si})(kT/q)$ which gives, from (A-13):

$$E_S^* = \frac{Q_D/2}{\varepsilon_{si}} + \frac{1}{2}\frac{kT}{q}\frac{C_{ox}}{\varepsilon_{si}}$$

$$\frac{n_S^*}{E_S^*} = \frac{C_{ox}}{2q}$$

From the definition of n_S^*, it comes:

$$\phi_S^* = 2\phi_F + \frac{kT}{q}\ln\left(\frac{C_{ox}}{4C_{si}}\left(1+\frac{kT}{q}\frac{C_{ox}}{Q_D}\right)\right)$$

Finally, Gauss' Law yields the threshold voltage:

$$V_{th} = 2\phi_F + V_{FB} + \frac{Q_D/2}{C_{ox}} + \frac{kT}{q}\left[\frac{1}{2} + \ln\left[\frac{C_{ox}}{4C_{si}}\left(1+\frac{kT}{q}\frac{C_{ox}}{Q_D}\right)\right]\right] \qquad \text{(A-14)}$$

Approximations made are very similar to those adopted for the previous model:
$E_S^* >> \Delta E$ is equivalent to $(Q_D/2) >> -(kT/q)C_{ox}$ and is always verified;
$t_{si}E_S >> 2(kT/q)$ gives $(Q_D/2) >> 2(kT/q)\left[C_{si} - (C_{ox}/4)\right]$ and is verified as soon as Q_D is large.

As for the BL model, with $Q_D >> (kT/q)C_{ox}$, (A-14) reduces to (A-10), the simplified form.

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Chapter III: High-temperature operation

Integrated circuits operating at elevated temperatures are of interest in various applications such as automotive, well logging, aircraft and spacecraft. Nuclear and space applications are also concerned. Bulk MOSFETs usually cease to function in the range 200...250°C due to excessive junction leakage currents and drift of the threshold voltage that first degrade speed or accuracy, increase the standby power dissipation, and finally could result in loss of functionality or in destruction by thermally activated latch-up. SOI circuits can be a viable alternative because they present three advantages over their bulk counterparts [1]:

- the absence of thermally-activated latch-up due to perfect isolation between adjacent devices,
- the reduction of leakage currents that results both from smaller drain junction areas and from a change in the physical leakage mechanism and,
- the smaller variation of the threshold voltage with temperature at least in thin film, fully depleted devices.

SOI SRAMs have demonstrated correct operation up to 300°C [2], devices were tested at 400°C [3] and ring oscillators have been measured up to 500°C [4] ! The motivation of this chapter is to prove, with discrete devices as well as on some digital circuits, that these electrical advantages remain or even are improved when using the GAA technology owing to the stronger gate control on the channel potential. Regular SOI and double-gate structures are compared with the same starting film thickness, gate oxide, threshold voltage and design. Temperature performances are measured by probing wafers placed on a temperature-regulated hot chuck allowing testing up to 320°C.

1. Device characteristics

Drain currents as a function of gate and drain voltages are depicted in Figure 3.1 for 3µm × 3µm GAA devices with temperature as parameter.

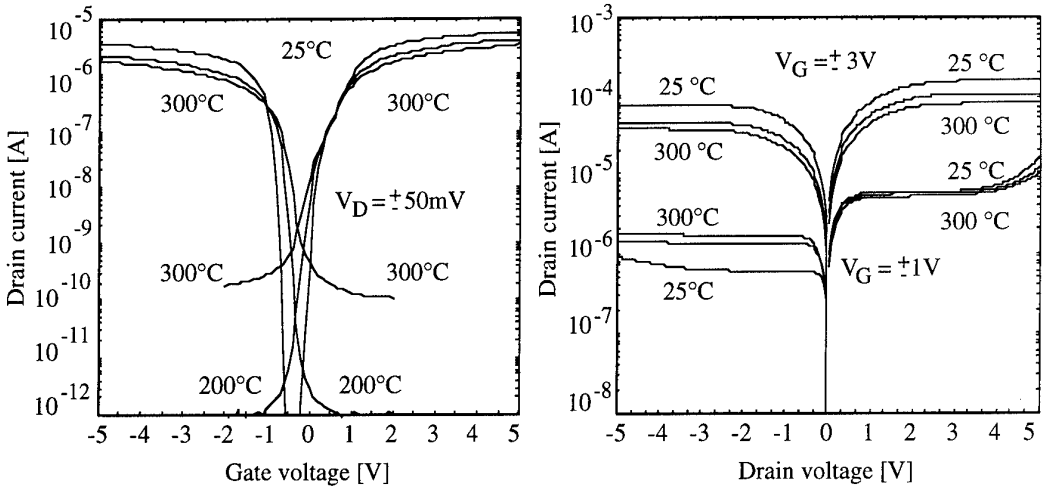


Figure 3.1: Drain current in GAA devices as a function of gate voltage (left) and drain voltage (right) at 25, 200 and 300°C.

Obviously, the curves are not strongly affected by temperature. A small reduction of the current drive capability as well as a small increase of leakage currents are nevertheless observable at 300°C. In Figure 3.1, the Zero Temperature Change (ZTC) point is well defined around V_{ZTC} = -1V for p-channel devices. With $|V_{ZTC} - V_{th0}|$ = 0.15V, and V_{th0} the room temperature threshold voltage, V_{ZTC} seems to be closer to V_{th0} than in regular SOI where $|V_{ZTC} - V_{th0}|$ is usually around 0.4V. On the other hand, the current in n-type transistors is approximately independent on temperature in a wide range of gate voltages from 0.3V to 0.8V, as clearly observed in Figure 3.1 as well. This range corresponds to the transition region where the edge transistor is already turned on while the main transistor is still turned off. The current is probably maintained constant due to some compensation between the temperature variation of edge and main threshold voltages. In the following, electrical parameters (threshold voltage, leakage current, transconductance and output impedance) will be reviewed successively in detail.

1.1. Threshold voltage

At the light of simple theoretical models, it will be shown that very small threshold voltage drifts with temperature are expected in GAA structures. Experimental evidence of reduced GAA threshold voltage roll-off is then presented.

• A generic rough expression for the threshold voltage of n-channel inversion-mode MOSFETs (bulk, SOI, GAA) is:

$$V_{th} \approx \phi_{ms} - \frac{Q_{ox}}{C_{ox}} + 2\phi_F + \frac{Q_D}{C_{ox}} = \frac{\pm E_g}{2} - \frac{Q_{ox}}{C_{ox}} + \phi_F + \frac{Q_D}{C_{ox}}$$

We recall that ϕ_{ms} is the work function difference between gate and semiconductor (gates being made of N^+ or P^+ polysilicon). $\phi_F = (kT/q)\ln(N_A/n_i)$ is the Fermi potential, Q_D is the depletion charge controlled by the gate and C_{ox} is the capacitance associated to the gate oxide. In bulk devices, $Q_D = qN_A x_{d\,max} = \sqrt{qN_A 4\varepsilon_{si}\phi_F}$ [5] where x_{dmax} is the maximum depletion depth with the surface in strong inversion. In

fully-depleted (FD) SOI devices, $Q_D \approx (qN_A t_{si}/n)$ [6] where n is ranging between 1 and 2 depending on oxide charges and back-gate bias conditions. In FD GAA devices, $Q_D = (qN_A t_{si}/2)$ due to the symmetrical charge sharing between front and back gates (Chapter II). For simplification, we assume that Q_{ox}, the charge density in the gate oxide, shows no temperature dependence while surface states at the Si/SiO_2 interfaces are omitted.

Since the intrinsic carrier concentration is very sensitive to temperature:

$$n_i(T) = n_{io} T^{3/2} e^{-E_g/2kT}$$

with $n_{io} = n_i(300K)$ [6], the Fermi potential varies with temperature. Assuming that E_g is constant (it actually varies by 10% between room temperature and 300°C [7]), one easily obtains [6]:

$$\frac{\partial \phi_F}{\partial T} = \frac{k}{q}\left[\ln(N_A) - \ln(n_{io}) - \frac{3}{2}(1+\ln(T))\right]$$

In bulk devices, Q_D is modified by temperature while Q_D is constant in FD SOI/GAA transistors. Subsequently, the temperature sensitivity of the threshold voltage is different in bulk or in SOI/GAA devices:

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial \phi_F}{\partial T}\left[1 + \frac{q}{C_{ox}}\sqrt{\frac{\varepsilon_{si} N_A}{kT\ln(N_A/n_i)}}\right] \approx -2...3\text{mV/K} \quad \text{in bulk devices and}$$

$$\frac{\partial V_{th}}{\partial T} \approx \frac{\partial \phi_F}{\partial T} \approx -0.6...0.8\text{mV/K} \quad \text{in SOI/GAA transistors.}$$

Numerical values are indicative and strongly depend on n_{io} and on the gate oxide thickness in bulk. Nevertheless, the mere comparison of these two expressions shows that $(\partial V_{th}/\partial T)$ could be 2 to 3 times smaller in thin SOI/GAA devices than in bulk transistors as long as they operate in fully depleted mode. Because of its dependence on ϕ_F, the maximum depletion width x_{dmax}, controlled by the gate, decreases with temperature. As a consequence, above a critical temperature T_k, the SOI/GAA film is no longer fully depleted and the temperature dependence of the threshold voltage becomes similar to that observed in bulk devices. T_k can be approximately extracted from the following relationship:

$$x_{d\,max} = \sqrt{\frac{4\varepsilon_{si}\frac{kT}{q}\ln\left(\frac{N_A}{n_i(T_k)}\right)}{qN_A}} \geq \alpha t_{si}$$

with t_{si} the silicon film thickness. In SOI, $\alpha = 1$ when the back interface is accumulated and tends to 0.5 at increasing back-gate voltage. In double-gate devices, the depletion arises from both sides of the silicon film so that α reaches the minimum value 0.5. GAA devices therefore provide minimum threshold voltage sensitivity up to the highest temperature. Figure 3.2 compares the critical temperature of GAA transistors ($T_{k,GAA}$) and the worst case (minimum) critical temperature of SOI devices obtained with

accumulation at the back interface ($T_{k,SOI,acc}$). T_k is plotted as a function of the silicon film thickness with the doping concentration as parameter. The adopted variations for n_i and E_g are reported in [7].

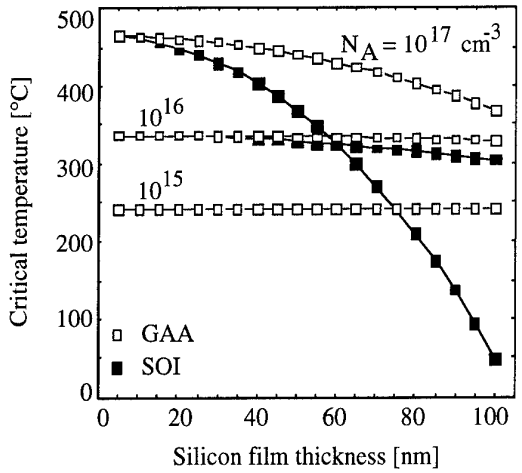


Figure 3.2: Maximum temperature still ensuring full depletion operation in SOI and GAA devices as a function of silicon film thickness with doping concentration as parameter.
The back interface is accumulated in SOI devices.

At light doping concentration, the critical temperature is nearly the same for both SOI and GAA devices and is close to 250°C. When the doping level is increased, the improvement of T_k provided by the GAA structure is appreciable. For example, with $N_A = 10^{17}cm^{-3}$ and t_{si} around 75...85nm, $T_{kSOI,acc}$ is only around 210...240°C while T_{kGAA} reaches the range 400...410°C. Reciprocally, to ensure $T_k > 300°C$ with $N_A = 10^{17}cm^{-3}$, SOI devices have to be thinned down to 65nm while 100nm-thick GAA transistors still fulfill the condition.

The experimental confirmation is provided in Figure 3.3 where V_{th} is plotted as a function of temperature. Threshold voltages were extracted using the maximum transconductance change (TC) method (Chapter II).

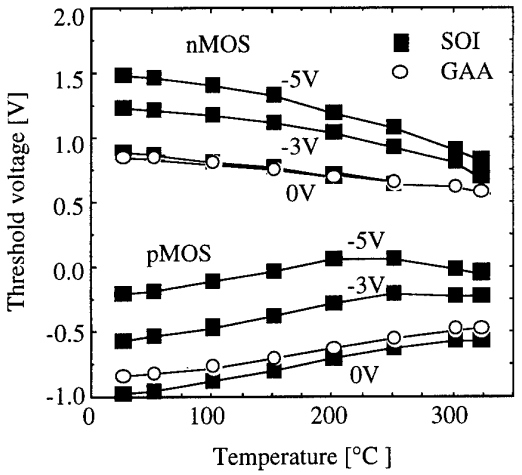


Figure 3.3: N- and p-channel threshold voltages of SOI and GAA transistors as a function of temperature (in SOI, back-gate bias at -5V, -3V and 0V from top to bottom).

In both GAA and SOI nMOS devices, the temperature coefficient is less than -1mV/°C, value which is only slightly higher than the theoretical expectation. In GAA devices, the very flat temperature dependence is maintained up to 322°C. On the contrary, SOI transistors with back biases lower than -3V (back interface in accumulation) are no longer fully depleted above ~220°C which causes the V_{th}-curve to roll off.

• The turn on of accumulation-mode (AM) SOI devices has been studied by D. Flandre *et al.* [8]. The current first appears owing to the onset of the body conduction within the central quasi-neutral part of the film. For further more negative gate voltages, front and/or back interfaces end up in accumulation producing a second conduction component. From this model, the threshold voltage sensitivity can be derived as [9]:

$$\frac{\partial V_{th}}{\partial T} = -[1+\alpha]\frac{\partial \phi_F}{\partial T} \approx 1.1...1.3 mV / K$$

with α ranging from $(\varepsilon_{si} t_{ox})/(\varepsilon_{ox} t_{si} + \varepsilon_{si} t_{oxb})$ to $(\varepsilon_{ox} t_{si} + \varepsilon_{si} t_{ox})/(\varepsilon_{si} t_{oxb})$ depending on the back-gate bias. t_{oxb} is the buried oxide thickness. In AM SOI transistors, $(\partial V_{th}/\partial T)$ is hence predicted to be slightly larger than in EM FD devices but is still a factor of 2 smaller than in bulk devices. This has been experimentally verified [10]. Adapting the threshold voltage model of AM SOI devices to symmetrical structures, we obtain:

$$V_{th} = V_{FB} + \frac{qN_A t_{si}^2}{8\varepsilon_{si}}\left[1+\frac{C_{it}}{C_{ox}}\right] + \frac{qN_A t_{si}}{2C_{ox}}$$

for the body conduction onset. Surface accumulation turn on occurs later on, when the gate voltage decreases down to the flat-band voltage $V_{FB} = (\pm E_g/2) - \phi_F - (Q_{ox}/Cox)$. Usually, only the first threshold voltage corresponding to body conduction is observed, the accumulation surface current being marginal due to the very flat potential profile. Anyway, both V_{th} and V_{FB} exhibit the minimum same temperature dependence:

$$\frac{\partial V_{th}}{\partial T} \approx \frac{-\partial \phi_F}{\partial T} \approx 0.6...0.8 mV / K$$

as in EM FD devices. A very small threshold voltage variation of 1mV/°C is well observed experimentally in p-channel GAA devices up to 100°C in Figure 3.3. However, at 200°C, $(\partial V_{th}/\partial T)$ has increased up to 1.3mV/°C and merges with the behavior of regular AM SOI devices. This effect could reveal an inadequacy of the body threshold voltage definition at high temperature. The depletion approximation of Poisson's equation becomes indeed less accurate when the number of electron/hole pairs generated in the film becomes very large.

In regular SOI transistors, Figure 3.3 shows that V_{th} is strongly influenced by the back-gate-to-source voltage. As a consequence, the balance between n- and pMOS threshold voltages can be adjusted only for transistors having a common fixed source voltage and cannot be achieved for all devices inserted in complex circuits. Another strong advantage of the GAA structure is to be totally free of body effect (back-gate influence) since the active silicon is completely shielded by the surrounding gate. The threshold voltage is thus fixed by the doping level only for all operating conditions.

Furthermore, the temperature sensitivity of the n- and p-threshold voltages being approximately the same, measurements show that the symmetry between n and p transistor types could be maintained at least up to 320°C.

1.2. Leakage current

The leakage current at the reverse-biased body-drain junction of a n-channel transistor is approximately given by the sum of the diffusion component in the neutral region and the generation current in the depletion region [5]:

$$I_{leak} = q\left[\sqrt{\frac{D_n}{\tau_r}}\frac{n_i^2}{N_A}A + \frac{n_i}{\tau_g}V_W\right] \qquad (3\text{-}1)$$

with D_n the electron diffusivity, τ_r the electron recombination lifetime in the neutral body region and τ_g the effective generation lifetime in the space-charged region near the drain. A is the junction area of the neutral region at the drain edge. V_W is the volume of the depleted region controlled by the drain. In PD SOI, A is expressed as the product $[t_{si} - x_{d\,max}(L)]W$ [7] with W the device width, $x_{d\,max}(L) = \sqrt{(2\varepsilon_{si}(\phi_S + V_{DB})/qN_A)}$ the depletion depth at drain and V_{DB} the drain-to-substrate voltage. It should be noted that $\phi_S < 2\phi_F$ since the device is in the off-state. It is also generally assumed in SOI that $V_W = Wt_{si}W_i$ where W_i is a portion of the space-charged region where generation is maximum. V_W is slightly more complex if the generation current in the depleted body film is taken into account [7]. Although $x_{dmax}(L)$, W_i, D_n, τ_r and τ_g vary with temperature, the main temperature dependence of the leakage current I_{leak} is given by the intrinsic carrier concentration n_i.

In bulk and PD SOI devices, the diffusion of the carriers in the quasi-neutral region surrounding the drain junction plays a leading part, and the leakage current increases dramatically with temperature as n_i^2. In FD SOI, the quasi-neutral region is totally suppressed. As a consequence, at low temperature, the generation current dominates and the leakage now slowly varies with temperature as n_i. However, above a temperature of 100...150°C, to be determined experimentally, the diffusion component becomes preponderant, and the leakage increases with n_i^2 like in bulk. This change of leakage mechanism can be explained because the diffusion current increases more rapidly with temperature than the generation component, and also because devices are no longer FD above a critical temperature. On the other hand, it is worth to note that both A and V_W are much smaller in SOI than in bulk. Furthermore, the largest of all junctions, the well-junction is totally suppressed in SOI. As a consequence, extremely low leakage currents are observed in SOI transistors, two to three orders of magnitude lower than their bulk counterparts [1]. Improvement compared to bulk is also observed for accumulation-mode devices, *i.e.* with no junctions, because the leakage path is similarly reduced [1].

We have already shown that GAA devices remain FD up to a higher temperature than FD SOI transistors. The area of the neutral junction, if it exists, is also further reduced in GAA devices when compared to SOI devices due to the stronger depletion that arises from both sides of the film:

$$A_{GAA} = \left[\frac{t_{si}}{2} - x_{d\,max}(L)\right]W < 2A_{SOI}$$

As a result, lower diffusion leakage currents are expected. Now, if we assume the same generation current in FD GAA and SOI devices having the same film thickness, the ratio I_{ON}/I_{OFF} is improved at least by a factor of 2 in GAA owing to double-gate conduction. Finally, it has been reported that extreme thinning of the silicon film in SOI adversely affects the room temperature leakage due to low activation energy leakage mechanisms occurring at the defective back interface [11]. GAA devices should be free of such defect-activated generation since the back interface is of same high quality than the top interface. As a result, GAA transistors should present lower room-temperature leakage currents than their SOI counterparts, this effect being preserved or even reinforced at high temperature.

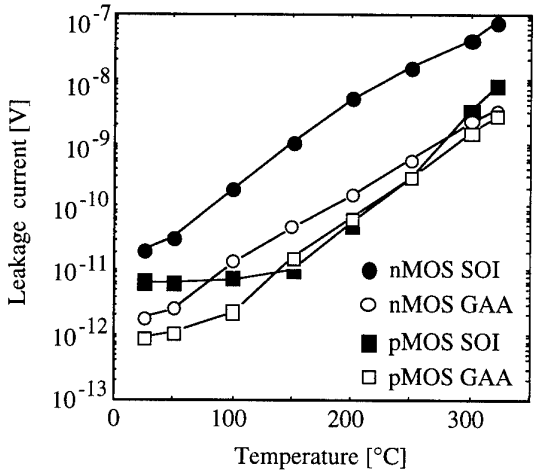


Figure 3.4: N- and p-channel leakage current of SOI and GAA transistors as a function of temperature (with V_G = -1.5 and 1.5V and V_D = 1 and -1V respectively).

Figure 3.4 compares the leakage current measured up to 322°C in n-type FD EM SOI and GAA transistors as well as in p-type AM SOI and GAA devices. V_G = -1.5(1.5V) and V_D = 1(-1V) in n(p)-channels. I_{ON}/I_{OFF} ratios in excess of 10000 at 200°C and 100 at 300°C are obtained. It can be seen, as expected, that leakage currents as well as their temperature sensitivity are slightly reduced when using the GAA technology.

1.3. Transconductance

Figure 3.5 depicts the drop of the maximum transconductance $g_{m,max}$ observed in SOI and GAA n- and p-channel devices as a function of temperature. $g_{m,max}(T)$ decreases as a result of the reduction of the phonon-scattering-limited surface mobility. At room temperature, the transconductance g_m in GAA transistors is known to give a higher maximum value than in SOI devices. The benefit is at least a factor of 2 due to the action of front and back transistors working in parallel. A further higher gain is obtained if the device exploits volume conduction with enhanced mobility (Chapter II). Figure 3.5 clearly shows that the transconductance enhancement provided by the GAA structure subsists at high temperature in both n- and p-channel MOSFETs. However, SOI and

GAA maximum transconductances cannot be directly compared because, first of all, $g_{m,max}$ is not necessarily obtained at the same gate voltage overdrive V_G-V_{th} for all measurements (which is recommended for rigorous comparison as shown in Chapter II). Furthermore, the impact of series resistances on $g_{m,max}$ is not identical in SOI and GAA devices since series resistances are expected to be the same in both structures but approximately twice the SOI current flows through GAA transistors.

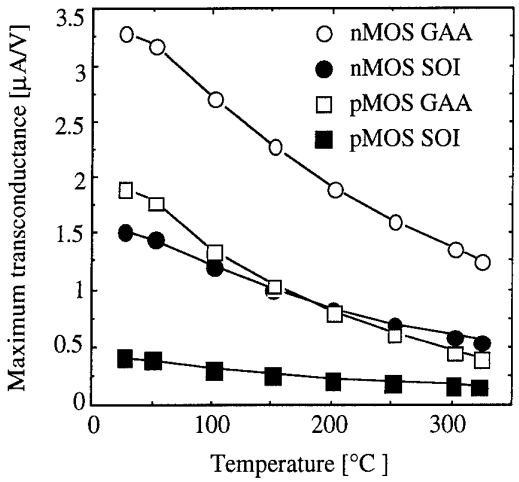


Figure 3.5: N- and p-channel maximum transconductance of SOI and GAA transistors as a function of temperature.

In order to properly separate the temperature evolution of 'pure' mobility μ (only related to the amount of interface states) and intrinsic mobility attenuation factor θ' (due to vertical electric field) from the influence of source/drain series resistances $R_{sd} = R_S + R_D$, we use the method proposed in [12] based on the following linear approximation:

$$g_m = \frac{C_{ox}WV_{DS}}{L}\frac{\mu}{\left[1+\theta(V_G-V_{th})\right]^2} \approx \frac{\mu C_{ox}WV_{DS}}{L}\left[1-2\theta(V_G-V_{th})\right] \quad (3\text{-}2)$$

where $\theta = \theta' + R_{sd}(\mu C_{ox}W/L)$. In SOI, R_{sd} can be evaluated using the Terada, Muta and Chern (TMC) method [13,14] based on current measurements in transistors with various drawing lengths. Using 20, 10, 5, 3, 2 and 1.5µm-long devices, the following temperature sensitivity of R_{sd} is obtained:

$$R_{sd}(T) = R_{sd0}\left[1+0.001(T-T_0)\right]$$

with the subscript 0 indicating room temperature values. The same TMC method would be much less precise in the GAA case where only 3, 2 and 1.5µm-long devices are available. Therefore, we assume that $R_{sd}(T)$ is identical in GAA and SOI devices since series resistances should be the same in both structures. $V_{th}(T)$ is extracted from Figure 3.3. $\theta(T)$ and $\mu(T)$ are respectively obtained from the slope and the intercept at $V_G = V_{th}(T)$ of the best linear regression to the straight portion of the $g_m(T)$ curve above threshold. $\theta'(T)$ emerges when deducing the contribution of $R_{sd}(T)$ from $\theta(T)$. Results are plotted in Figure 3.6 with $W_{GAA} = 2W_{SOI}$.

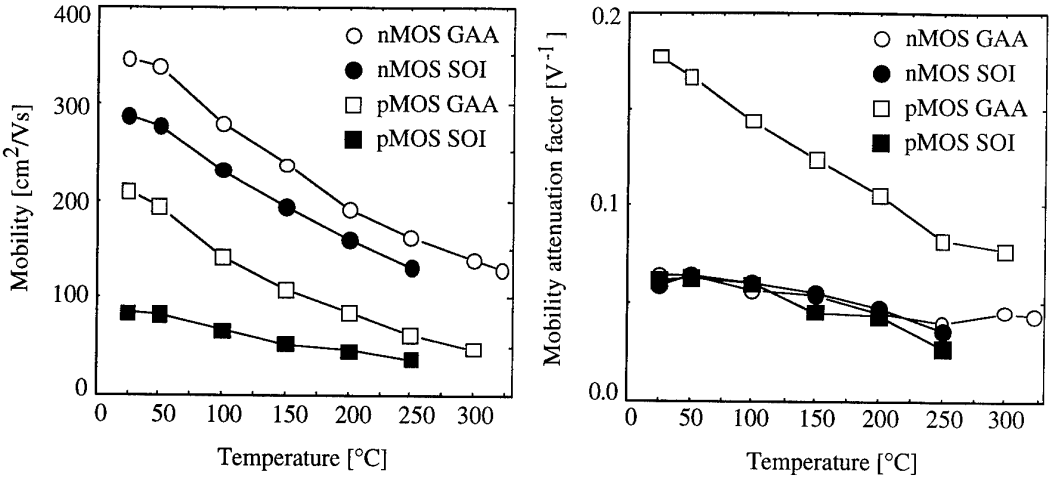


Figure 3.6: Pure mobility (left) and intrinsic mobility attenuation factor θ' (right) in n- and p-channel SOI and GAA transistors as a function of temperature. $W_{GAA} = 2W_{SOI}$

In SOI devices, the classical model $\mu(T) = \mu_0(T/T_0)^{-m}$ is valid for both n- and p-channel devices with m in the range 1.6...1.8 as observed elsewhere [15]. Since a correct fitting to the n-channel GAA mobility curve is obtained with m = 1.7, GAA and SOI n-channel mobilities are governed by the same temperature dependence. As a result, the ratio $M_n = \mu_{nGAA}/2\mu_{nSOI}$ remains nearly perfectly constant around 1.2 throughout the whole temperature range. The relatively low value of M_n indicates that volume inversion is modest above threshold due to the high doping level of the film. Now, the exponent m of the classical $\mu(T)$ model must be increased up to 2.5 to obtain a correct fitting to the temperature dependence of the p-channel GAA mobility. As a consequence, in p-channels, $M_p = \mu_{pGAA}/2\mu_{pSOI}$, which is close to 2.5 at room temperature, drops to about 1.6 at 250°C. This could be an indication that body conduction is extremely important in p-channel AM GAA devices at room temperature and that either the surface accumulation conduction becomes preponderant or the volume mobility decreases towards the surface value at increasing temperature. As indicated in the right part of Figure 3.6, the intrinsic mobility attenuation factor due to transverse electric field θ' is about the same in n- and p-channel SOI transistors as well as in n-channel GAA transistors, and slightly decreases with temperature. The totally different behavior of p-channel GAA devices is again clearly visible. More and systematic measurements should be performed in order to confirm these data.

1.4. Output impedance

Extending the definition of the Early voltage of bipolar transistors, the output impedance is represented by $V_{EA} \approx \left[\partial \ln(I_D)/\partial V_D\right]^{-1}$. Since V_{EA} slightly depends on the drain voltage, the maximum value is extracted from measurements. As shown in Figure 3.7, V_{EA} is larger in GAA transistors than in SOI devices at all temperatures. The reason is the better control of the active channel from front and back sides of the film which results in a reduction of the depletion region controlled by the drain. The average enhancement offered by GAA devices starts from more than 3 at room temperature and is still superior to 2 at 322°C. V_{EA} increases with temperature in SOI owing to reduced mean free path of carriers and hence to reduced impact ionization [1]. The GAA behavior

is difficult to interpret because it is neither stable nor identical for p- and n-channel transistors: accumulation-mode pMOSFETs present an increase(chaotic decrease) of V_{EA} below(above) 200°C while inversion-mode nMOSFETs show a steady decrease of V_{EA} with temperature. The output impedance should therefore be investigated in more detail since it is a critical parameter for analog applications.

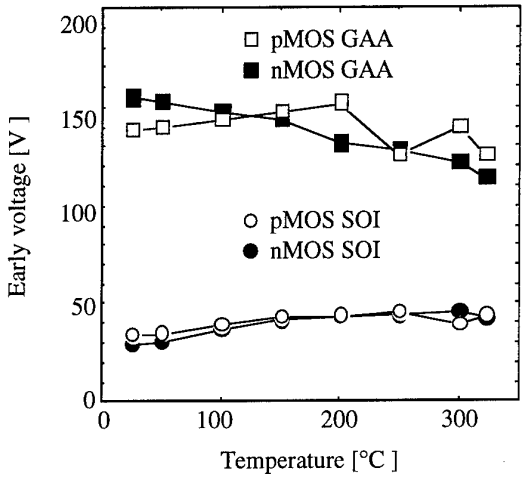


Figure 3.7: N- and p-channel maximum Early voltage of SOI and GAA transistors as a function of temperature.

2. Circuit performance

When logic gates are considered, leakage in SOI compares even more favorably to bulk than could be expected from individual device performance. Indeed, no current is allowed to flow towards the substrate in an SOI gate so that the internal leakage is limited by the least leaky device in a series association of transistors [16]. As will now be shown, simple logic circuit operation also confirms the superiority of the GAA technology over its SOI counterpart.

2.1. CMOS inverters

The transfer curves of both GAA and SOI CMOS inverters exhibit no important degradation at high temperature up to 320°C (Figure 3.8). The switching voltage remains more stable in GAA circuits due to the symmetrical and remarkably weak variation of the n- and p-channel threshold voltages. The reduced drive capability of the "on" device (due to reduced mobility) and the slightly increased leakage current of the "off" device reduce the output range from only a few millivolts.

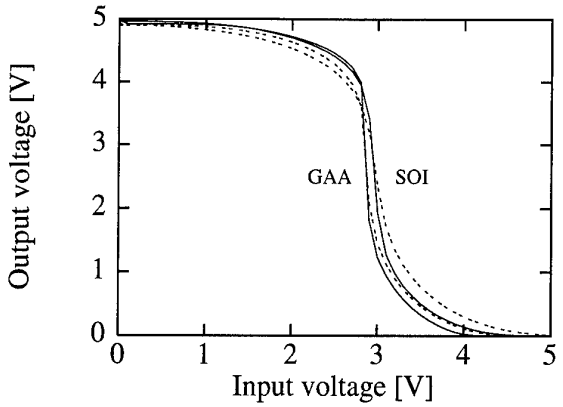


Figure 3.8: Static transfer characteristics of GAA and SOI inverters at 25°C (plain curve) and at 300°C (dashed curve).

2.2. Maximum operating frequency

We investigate here the maximum operating frequency F_{max} of an inverter followed by a gate transistor as shown in Figure 3.9. Such a circuit could be used as write circuit in an SRAM for example. F_{max} is here defined by the frequency of the input clocking signal still giving an output swing of 90% of the static output range. In SRAMs, this circuit should feed a memory cell, presenting an internal capacitance of approximately 0.1pF. In Figure 3.9, F_{max} is evaluated when the inverter charges and discharges a loading capacitance of 15pF (corresponding to the input capacitance of the scope) which explains why very small values of F_{max} are obtained. The GAA version is faster than the SOI circuit due to higher n- and p-type transconductances. F_{max} decreases with temperature as expected from the evolution of the maximum transconductance shown in Figure 3.5. Although the simple circuit below cannot be helpful to deduce the operating frequency that could be achieved by an actual GAA SRAM, it clearly shows that, if the GAA technology provides any speed advantage, this advantage survives at very high temperature.

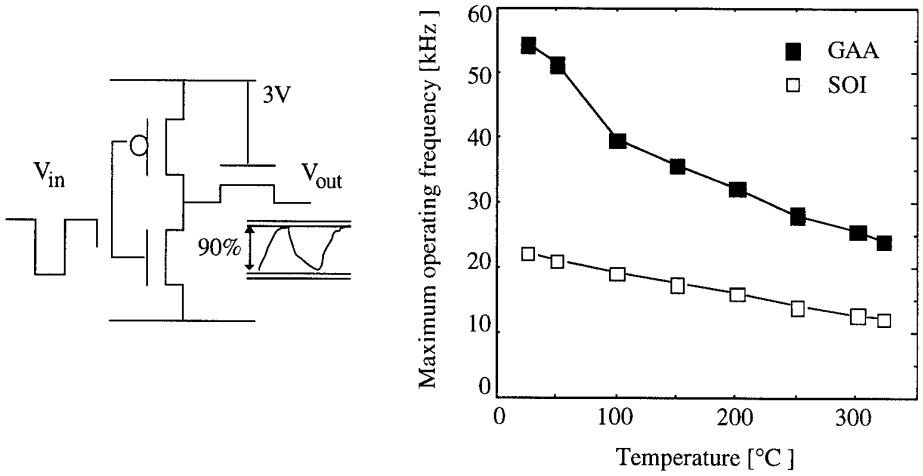
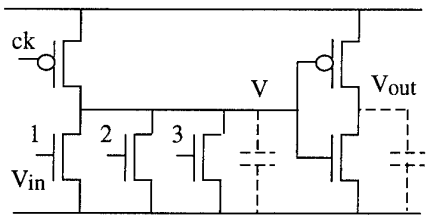


Figure 3.9: Maximum operating frequency of write circuits for SRAMs in GAA and SOI technologies as a function of temperature (loading capacitance of about 15pF).

2.3. Dynamic circuits

Dynamic circuits must be periodically refreshed because leakage currents alter the information stored. Therefore, it is expected that the maximum holding time before refreshing decreases with increasing temperature. The holding time capability has been evaluated with a 3-input dynamic decoder operated as follows (Figure 3.10). The three inputs are grounded. The internal capacitance is first precharged with the clocking signal ck at 0V, giving a low output voltage V_{out}. Next, the circuit is placed in holding mode with ck at the supply voltage (V_{dd} = 3V). The internal node inevitably slowly discharges through off-biased input nMOS transistors. The holding time HT is measured from the transition of ck and is defined as the time required for V_{out} to reach 10% of V_{dd}. Figure 3.10 shows that, at low temperature, the GAA holding time is slightly lower than in SOI because the initial n-channel threshold voltage is lower, implying a larger leakage at V_G = 0V. At high temperature, approximately the same performance is reached with both technologies, which proves that GAA transistors undergo less degradation. The holding time decreases by about one order of magnitude between room temperature and 300°C: HT ≅ 25µs at 25°C and 2µs at 320°C. Correct operation is therefore possible at high temperature if the refreshing occurs at a frequency superior to about 1MHz which should be more easily obtained at 300°C with the GAA technology since the large driving capability is maintained up to a high temperature (Figure 3.9) (this supposes no dramatic increase of the parasitic capacitances in the GAA structure).



	Vin				
	ck	1	2	3	Vout
Initialization	0	0	0	0	0
Holding	1	0	0	0	0
Error	1	0	0	0	1

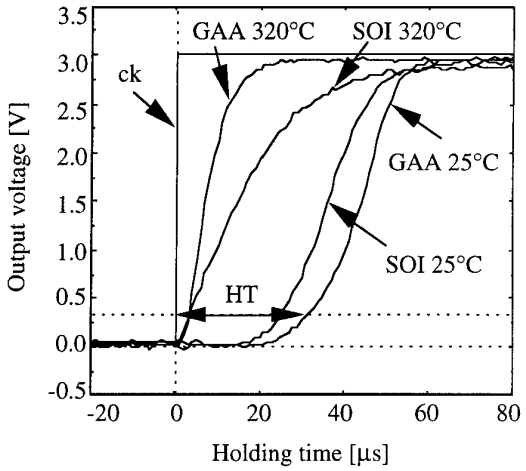


Figure 3.10: Output voltage of a dynamic circuit as a function of time with temperature as parameter. The holding time is noted HT.

3. Conclusions

Characteristics of similar GAA and SOI discrete devices and simple digital circuits were compared at high temperature. Better performance is obtained with the GAA process. The minimum threshold voltage sensitivity with temperature of FD EM n-channel devices is maintained at least up to 322°C in GAA while it vanishes at 200°C in SOI with the back interface in accumulation. The threshold voltage roll-off of AM p-channel devices is also smaller in GAA than in SOI up to 150°C. Also, the ratio I_{ON}/I_{OFF} is at least a factor of 2 larger in the GAA case throughout the whole temperature range.

Those improvements can be explained because, in GAA devices, the film-depletion is induced simultaneously by front and bottom parts of the surrounding gate. It was also shown that the large current driving capability of the GAA structure is preserved at high temperature. Those measurements prove the aptitude of GAA devices for static operation up to 322°C and probably beyond. GAA circuits also seem to present a strong potential for dynamic operation though this point should be confirmed. Now that we have investigated the behavior of SOI and GAA circuits in a heated ambiance, we will focus on self-heating effects occurring when large power is dissipated in the devices.

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Chapter IV: Self-heating effect

Smart power applications cover a big market related to automotive applications and other transportation systems (airplanes, suburban railways). Power devices are also found in high frequency applications, such as satellite communications and mobile transceivers, where the high speed of SOI is highly appreciated. However, severe problems arise in power SOI devices due to the self-heating. The buried dielectric isolation has a poor thermal conductivity which leads to an increase of the channel temperature when large power is involved. As a result, the device mobility is reduced (Chapter III) which decreases the maximum drain saturation current and causes a negative differential conductance in saturation [1,2,3,4]. Thinning the buried oxide has been proposed to enhance the heat flow towards the substrate [5] but results in loss of the SOI speed advantage due to the increase of parasitic capacitances. The buried oxide thinning could also be detrimental to achieve very high breakdown voltages [6]. For the first time, it will be highlighted that the use of GAA devices is favorable to reduce the self-heating problem. Indeed, in GAA transistors, the buried oxide is removed and replaced by a back polysilicon gate that benefits for a much larger thermal conductivity. This should substantially enhance the heat evacuation. On the other hand, GAA source and drain regions still lie on the thick buried oxide layer such that their parasitic capacitance with the substrate is kept small.

At first, this chapter presents the calculation of the global thermal conductance of the GAA structure. A general detailed discussion of the heat transfer as a function of the buried oxide thickness in regular SOI devices is presented as well. Then, three independent experimental evidences of enhanced heat evacuation in GAA transistors are provided and analyzed. The expression of the thermal conductance obtained using the simple uniform temperature approximation qualitatively explains independent measurements.

1. General model for the scaling of the buried oxide

1.1. Notations

Longitudinal and transversal cross-sections of 3μm × 3μm SOI and GAA devices are schematically presented in the left and right portions of Figure 4.1 respectively. Physical dimensions are gathered in Table 4.1. SOI devices are separated from the top of the

underlying substrate, assumed to be the thermal ground plane, by the buried oxide layer (t_{oxb} = 390nm typically). From the heating viewpoint, GAA transistors are only separated from the substrate, in the channel region, by two thin layers of gate oxide (t_{oxf} = 30nm): one on the back of the channel, one on the bottom of the cavity. The gap between the oxide layers is filled by the back polysilicon gate ($t_{backgate} = t_{oxb}-1.32t_{oxf}$).

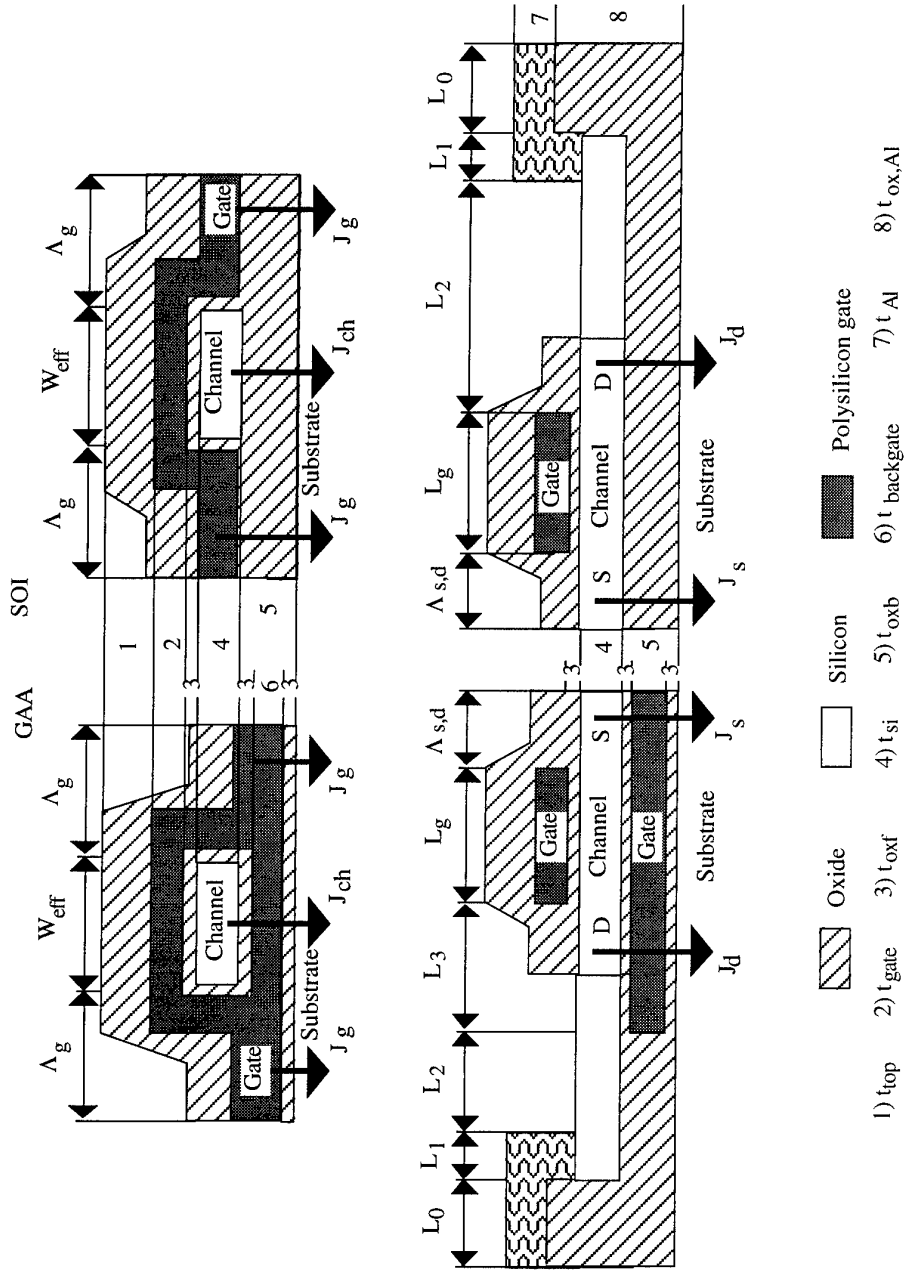

Figure 4.1: Transversal and longitudinal cross-sections of mesa SOI and GAA devices. The relative proportions of the physical dimensions, listed in Table 4.1, are not respected.

Table 4.1: Geometric parameters of SOI and GAA devices.

Layer	Notation	[µm]	Layer	[µm]	SOI	GAA
Passivation oxide	t_{top}	1	Aluminium line	L_0	50	50
Polysilicon gate	t_{gate}	0.34	Aluminium/Si contact	L_1	12	12
Poly back gate	$t_{backgate}$	0.36	SiN^+	L_2	4	2.5
Gate oxide	t_{oxf}	0.030	Cavity overetch	L_3	_	1.5
Silicon film	t_{si}	0.075	Effective width	W_{eff}	2.75	2.35
Buried oxide	t_{oxb}	0.390	Effective length	L_{eff}	2.4	2.4
Aluminium line	t_{Al}	1	Physical length	L_g	2.85	2.85
Oxide below Al	$t_{ox,Al}$	0.89				

1.2. Analytical model

The power P, uniformly dissipated in the device, is evacuated through the channel, source/drain and gate regions as sketched in Figure 4.1:

$$P = J_{ch} + J_{s,d} + J_g$$

with J_{ch}, $J_{s,d}$ and J_g the heat flows through the different regions. With G_{ch}, $G_{s,d}$ and G_g the thermal conductances per unit area of channel, source/drain and gate regions respectively, and ΔT the temperature elevation of the channel, the power can be expressed as [2]:

$$P = W_{eff} L_{eff} \left[G_{ch} + \frac{2\Lambda_{s,d}}{L_{eff}} G_{s,d} + \frac{2\Lambda_g}{W_{eff}} G_g \frac{\Delta T_g}{\Delta T} \right] \Delta T \qquad (4\text{-}1)$$

W_{eff} and L_{eff} are the effective width and length of the device, $\Lambda_{s,d}$ and Λ_g are the temperature decay lengths in the source/drain and gate regions and ΔT_g is the temperature elevation of the gate. Usually, ΔT is supposed to be uniform in the channel which is a fairly good approximation at low drain voltage or when the channel is short compared to $\Lambda_{s,d}$ [2,3]. This assumption is not verified in 3µm × 3µm SOI and GAA devices operated in saturation as illustrated by Figure 4.2. This figure depicts the lattice temperature distribution, obtained by two-dimensional device simulation, along the channel (right part) and along a vertical cross-section near the drain (left part). Two different boundary conditions on top of the front gate attempt to simulate the impact of the heat flow along the third dimension (BC1-BC2). Though the temperature elevation strongly depends on proper boundary condition, it is clear that the temperature profile is not constant along the channel. Most of the temperature increase is found near the pinch-off region where the electric field is the highest. This non-uniformity of the temperature profile is even more pronounced in the GAA case where self-heating is very small. However, for simplicity, we still maintain the assumption of constant ΔT. We also assume uniform ΔT_g despite of the fact that some temperature gradient could exist between top and bottom parts of the surrounding gate (Figure 4.2, left part). This should be confirmed by three dimensional simulations.

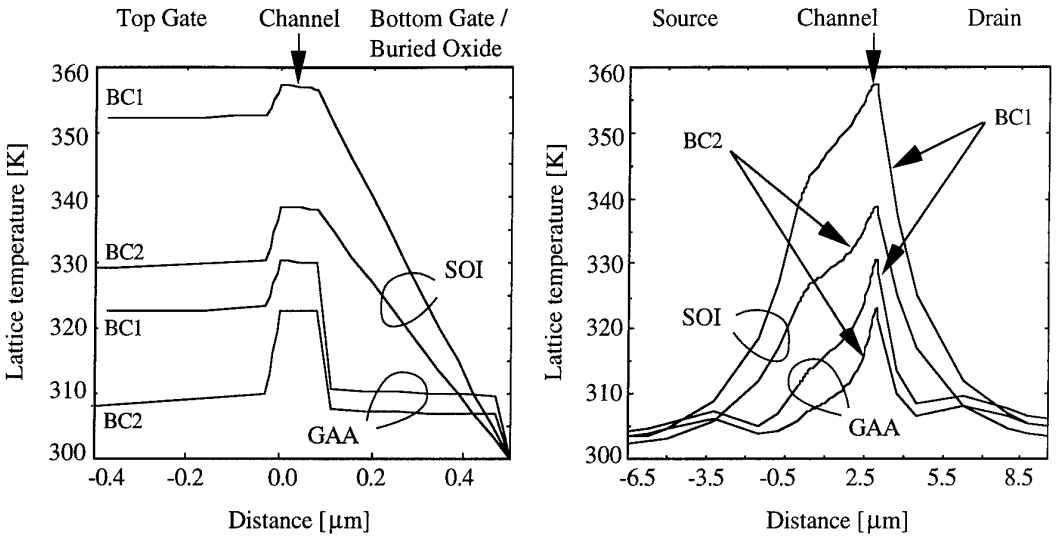

Figure 4.2: Two-dimensional numerical simulations of the lattice temperature distribution for P ≈ 3mW and 6mW in SOI and GAA devices respectively (V_G = 6V, V_D = 8.5V).
Left: Vertical cross-section at the drain edge of the channel (indicated by the arrow in the right part).
Right: Horizontal cross-section in the middle of the film (indicated by the arrow in the left part).
BC1 and BC2 refer to worst case and realistic boundary conditions on top of the front gate.

The different terms of relationship (4-1), summarized in Table 4.3, will now be discussed in detail. The thermal conductivities κ adopted for the different materials are listed in Table 4.2. These values are supposed to be independent of temperature although a slight dependence has been reported [5,7]. As far as κ_{SiO_2} is concerned, we have chosen the value proposed in References [2,3] which nevertheless seems to be 20% to 30% above the most recent experimental measurements [7]. We have adopted the same κ_{SiO_2} value for both the thermally grown gate oxide and the SIMOX buried oxide, despite of their different nature and defects.

Table 4.2: Physical properties of different materials.

Material	Thermal Conductivity κ [W/(cmK)]	Density ρ [g/cm³]	Specific Heat c [cal/(gK)]
SiO_2	0.014	2.2	0.71
Si	1.5	2.3	0.17
SiN^+	0.75	2.3	0.17
Al	2.4	–	–

• The heat flow through the channel region

In SOI devices, the channel thermal conductance per unit area $G_{ch,SOI}$ is simply inversely proportional to the buried oxide thickness $G_{ch,SOI} = \kappa_{SiO_2}/t_{oxb}$. In GAA devices, $G_{ch,GAA} = \kappa_{SiO_2}/(2t_{oxf}\beta)$ with $\beta = \left[1+\kappa_{SiO_2}t_{backgate}/\left(\kappa_{SiN^+}2t_{oxf}\right)\right]$. The term β takes into account the presence of the back-gate and is close to unity since κ_{SiN^+} (the thermal conductance of the back-gate) is about two orders of magnitude larger than κ_{SiO_2} (Table 4.2). Hence, as expected, the heat flow is mostly limited by the two thin

oxide layers. The area of the channel heat flow is given by the product of the device effective dimensions.

Table 4.3: Summary of thermal resistances and thermal conductances per unit area.

$G_{ch,GAA}$	$\frac{\kappa_{SiO2}}{2\,t_{oxf}\,\beta}$	β	$1+\frac{\kappa_{SiO2}}{\kappa_{SiN^+}}\frac{t_{backgate}}{2\,t_{oxf}}$
$G_{ch,SOI}$	$\frac{\kappa_{SiO2}}{t_{oxb}}$	R_{SiN^+}	$\frac{1}{\kappa_{SiN^+}\,t_{si}}$
$G_{Al/Si,ct}$	$\frac{2\kappa_{SiO2}}{t_{oxb}}$	$R_{Al/Si,ct}$	$\frac{1}{2\left[\kappa_{Al}\,t_{Al}+\kappa_{SiN^+}\,t_{si}\right]}$
$G_{Al,line}$	$\frac{2\kappa_{SiO2}}{t_{ox,Al}}$	$R_{Al,line}$	$\frac{1}{2\kappa_{Al}\,t_{Al}}$
$G_{g,GAA}$	$2\beta G_{ch,GAA}$	R_g	$\frac{1}{\kappa_{SiN^+}\,t_{gate}}$
$G_{g,SOI}$	$\frac{t_{oxb}}{t_{oxb}+2.3t_{si}}\,G_{ch,SOI}$	G_{chf}	$\frac{\kappa_{SiO2}}{t_{oxf}}$

• The heat flow through the source and drain regions

As shown in Figure 4.1, the source/drain regions outside the channel include different portions. The first three portions are common to SOI and GAA structures and correspond successively to the aluminum line, the aluminum/silicon contact and the N^+ silicon region lying on the thick buried oxide layer. The last portion is specific to GAA devices and consists of N^+ silicon above the back portion of the gate. The length of the successive portions L_i with $0 \le i \le i_{max}$ are listed in Table 4.1 with i_{max} equal to 2 and 3 in SOI and GAA transistors, respectively. To evaluate the heat flow through the source and drain areas, the different portions must be combined in a distributed transmission line model [2] as depicted in Figure 4.3.

The lateral thermal resistances R_i and vertical thermal conductances per unit area G_i of all portions i are summarized in Table 4.3. G_i equals $\left(W_i\kappa_{SiO_2}\right)/\left(W_{eff}t_{oxi}\right)$ where t_{oxi} is the thickness of the oxide layer separating portion i from the substrate and W_i is the width of portion i. In our process, the minimum size of a contact hole is identical to the channel width (3µm) and the contacting layers oversize the contact area by 1.5µm on each side (Figure 1.7). As a result, the aluminum line and the silicon layer in the contact area are twice as large as the channel region: $W_0 = W_1 = 2W_2$. R_i is given by $W_{eff}/\left(W_i\kappa_i t_i\right)$ where t_i, and κ_i are the thickness and the thermal conductivity of portion i respectively.

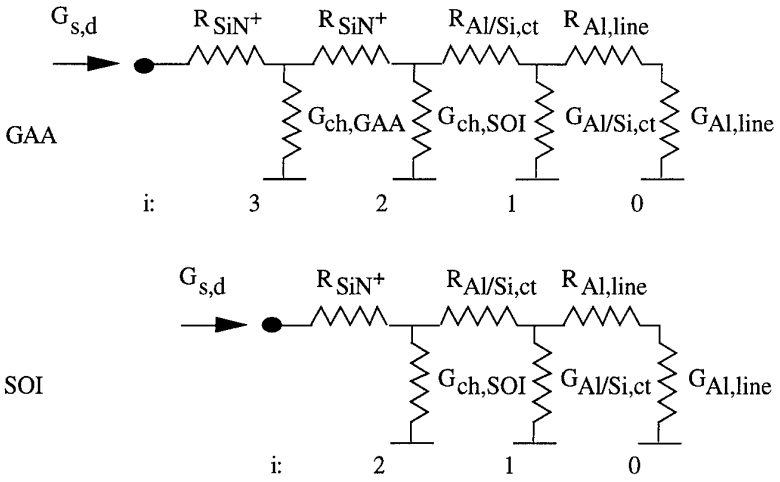

Figure 4.3: Distributed transmission lines forming the source/drain regions in GAA (top) and SOI (bottom) devices. i is the index of the different portions.

The equivalent thermal conductance of the transmission line at the channel edge $G_{s,d}$ equals $G_{imax}\tilde{G}_{i\,max}$ with $\tilde{G}_{i\,max}$ obtained recursively from i = 0 to i_{max} using [2]:

$$\tilde{G}_i = \frac{\sinh\left(\frac{L_i}{\Lambda_i}\right) + \gamma_{i,i-1}\tilde{G}_{i-1}\cosh\left(\frac{L_i}{\Lambda_i}\right)}{\cosh\left(\frac{L_i}{\Lambda_i}\right) + \gamma_{i,i-1}\tilde{G}_{i-1}\sinh\left(\frac{L_i}{\Lambda_i}\right)} \quad \text{with} \quad \gamma_{i,i-1} = \sqrt{\frac{G_{i-1}R_i}{G_i R_{i-1}}} \quad \text{and} \quad \Lambda_i = 1/\sqrt{R_i G_i}$$

$\tilde{G}_{i\,max}$ is listed in Table 4.4 as a function t_{oxb} and $\tilde{G}_0$, the boundary condition of the problem. $\tilde{G}_{i\,max}$ is very close to unity because Λ_{imax} is smaller than L_{imax} and it depends only slightly on $\tilde{G}_0$. As a consequence, the distribution line analysis is ultimately not necessary and one may assume $G_{s,d} = G_{imax} = G_{ch}$ and $R_{s,d} = R_{imax} = R_{SiN^+}$. Hence, $R_{s,d}$ is the same in SOI and GAA transistors while $G_{s,d}$ is different in the two structures. As shown in Figure 4.1, the area of the source/drain heat flow in (4-1) is the product of the effective device width W_{eff} by twice the source/drain temperature decay length $\Lambda_{s,d} = 1/\sqrt{R_{s,d}G_{s,d}}$.

Table 4.4: Normalized thermal lateral conductance of source/drain regions at the channel edge for different boundary conditions and different oxide thicknesses.

	$\tilde{G}_{imax}$		
t_{oxb}	$\tilde{G}_0 = 0$	$\tilde{G}_0 = 1$	$\tilde{G}_0 = 1000$
30	1.0000	1.0000	1.0000
120	1.0000	1.0001	1.0001
210	1.0003	1.0003	1.0003
300	1.0012	1.0012	1.0012
390	1.0028	1.0029	1.0029
GAA	0.9976	0.9976	0.9976

• The heat flow through the gate region

The gate-to-substrate thermal conductance per unit area G_g is inversely proportional to the thickness of the field oxide under the gate: $G_g = \kappa_{SiO_2}/t_{oxg}$ with $t_{oxg} = t_{oxb}$ in mesa-SOI; $t_{oxg} = t_{oxb}+2.3t_{si}$ in LOCOS-SOI and $t_{oxg} = t_{oxf}$ in mesa-GAA. The area of the heat flow is here the product of L_{eff} by twice the temperature decay length in polysilicon $\Lambda_g = 1/\sqrt{R_g G_g}$. R_g is given in Table 4.3. ΔT_g is determined by the series combination of the channel-to-gate $G_{chf} = \kappa_{SiO_2}/t_{oxf}$ and the gate-to-substrate G_g thermal conductances: $\Delta T_g = G_{chf}/(G_{chf}+G_g)\Delta T$. Hence, ΔT_g is close to ΔT in SOI and to $0.5\Delta T$ in GAA.

1.3. Scaling of the buried oxide thickness

Introducing $\gamma = G_g/G_{ch}$, the uniform power dissipation P is finally rewritten as:

$$P \approx W_{eff}L_{eff}\left[G_{ch} + \frac{2\sqrt{G_{ch}}}{\sqrt{R_{s,d}L_{eff}}} + \frac{2G_{chf}}{\sqrt{R_g W_{eff}}}\frac{\sqrt{\gamma G_{ch}}}{G_{chf}+\gamma G_{ch}}\right]\Delta T$$
$$= \left[G_{Tch} + G_{Ts,d} + G_{Tg}\right]\Delta T \qquad (4\text{-}2)$$

This expression is very useful to discuss the scaling of the buried oxide thickness in SOI devices, since only one parameter strongly depends on t_{oxb}, namely $G_{ch,SOI} = \kappa_{SiO_2}/t_{oxb}$. The variation of γ is indeed a second-order effect, γ being exactly equal to unity (or close to unity as long as $t_{oxb} >> t_{si}$) as shown in Table 4.5. All other parameters are independent of t_{oxb}.

Table 4.5: Ratio between gate-to-substrate and channel-to-substrate thermal conductances.

Technology	$\gamma = G_g/G_{ch}$	
Mesa - SOI		$= 1$
LOCOS - SOI	$\dfrac{t_{oxb}}{t_{oxb}+2.3t_{si}}$	$\lesssim 1$
Mesa - GAA	2β	$\gtrsim 2$

The global thermal conductance $G_T = P/\Delta T$ is depicted in Figure 4.4 as a function of t_{oxb} for the LOCOS-SOI case. The individual contributions to the heat evacuation of channel G_{Tch}, gate G_{Tg} and source/drain $G_{Ts,d}$ regions as defined in (4-2) are shown as well (solid lines).

• G_{Tch}, which is a linear function of G_{ch}, follows a pure $(t_{oxb})^{-1}$-rule. In the log-log plot of Fig. 3, the channel contribution therefore increases with a slope equal to -1 when the buried oxide thickness is reduced.

• $G_{Ts,d}$ increases more slowly when t_{oxb} is scaled down, following a nearly exact $(t_{oxb})^{-0.5}$-rule. The reason is that the temperature decay length, and hence the area of the source/drain heat flow, shrink with $\sqrt{t_{oxb}}$.

• The slope of the equivalent thermal conductance for the gate region G_{Tg} is even smaller than -0.5. The deviation from the $(t_{oxb})^{-0.5}$-rule is due to the drop of the gate

temperature when t_{oxb} decreases down to values similar to t_{oxf}, and appears through the increasing importance of G_{ch} in the ratio $G_{chf}/(G_{chf}+\gamma G_{ch})$.

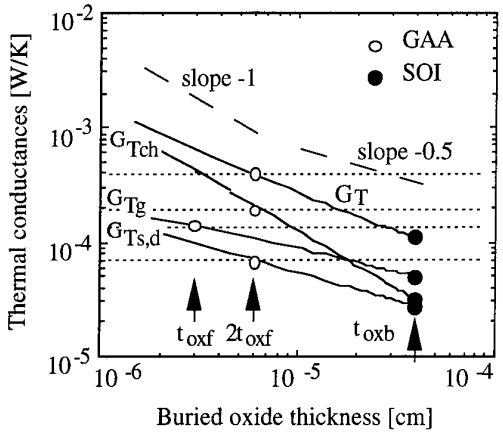

Figure 4.4: Global thermal conductance G_T and individual contributions of channel G_{Tch}, source/drain $G_{Ts,d}$ and gate G_{Tg} regions as a function of the buried oxide thickness in 3µm × 3µm devices. Solid lines are obtained for the LOCOS-SOI case. Horizontal dotted lines are for the mesa-GAA case.

It is also clear from Figure 4.4 that, for large t_{oxb}, the heat transfer through peripheral regions (G_{Tg} or $G_{Ts,d}$) is dominant so that the slope of the global thermal conductance G_T approaches -0.5 (as previously assumed in [3] but not clearly justified). In thin SOI films, the lateral heat transfer through the gate is usually more important than through the source/drain regions because the thickness of the gate t_{gate} is much larger than the film thickness t_{si} (and hence $R_g < R_{s,d}$). On the other hand, when the buried oxide thickness reaches very small values, the heat conduction underneath the channel prevails and the slope of G_T tends to -1. The smooth evolution of the slope between -1 and -0.5 depends on the relative importance of the heat flow through the three regions and hence on the device dimensions (Figure 4.4 is plotted for a 3µm × 3µm device). Since the channel dissipation scales with both W_{eff} and L_{eff} while the gate(source/drain) heat transfer only varies with $L_{eff}(W_{eff})$, the heat evacuation through peripheral regions should become more and more important when both device dimensions shrink. In this case, G_T should follow a $(t_{oxb})^{-0.5}$-rule down to smaller values of t_{oxb}.

1.4. Numerical predictions

The horizontal dotted lines of Figure 4.4 represent the different contributions to the heat flow in 3µm × 3µm GAA transistors. The intersections of dotted and solid lines clearly show that GAA devices behave nearly like SOI devices assuming that $t_{oxb} = 2t_{oxf}$, except for the gate contribution obtained with $t_{oxb} = t_{oxf}$. The gate contribution is indeed governed by γ which is close to 2 in GAA transistors rather than close to 1 as in SOI devices (Table 4.5). The dissipation in the gate area is nevertheless not dominant for such small values of equivalent t_{oxb} such that the experimental comparison of thermal conductances between GAA and SOI technologies corresponds to the scaling of the SOI buried oxide from t_{oxb} = 390nm (dark circles in Figure 4.4) to $2t_{oxf}$ = 60nm (open circles). The reduction of t_{oxb} down to $2t_{oxf}$ induces an indirect reduction of the temperature decay lengths in the source/drain and gate regions by a factor of about 3: $\Lambda_{s,d}$

= 1.25µm; Λ_g = 2.6µm in SOI devices while $\Lambda_{s,d}$ = 0.5µm; Λ_g = 0.75µm in GAA transistors. Assuming that W_{eff} = W and L_{eff} = L in both SOI and GAA transistors to really compare devices with the same sizes, the enhancement α of the total thermal conductance is:

$$\alpha = \frac{G_{T,GAA}}{G_{T,SOI}} = \frac{0.36}{1.12} = 3.2 \text{ , with } G_T \text{ expressed in [mW/K]}$$

As previously highlighted, α follows the buried oxide thickness to the n-th power with $-0.5 > n > -1$ and is larger than predicted by the usual square root-rule:

$$\sqrt{\frac{t_{oxb}}{2t_{oxf}}} (= 2.55) < \alpha < \frac{t_{oxb}}{2t_{oxf}} (= 6.5).$$

It is worth to note that the very small value of the equivalent buried oxide thickness t_{oxb} = 60nm provided by the GAA process is not currently available with the regular SIMOX technology. Moreover, the source/drain-to-substrate capacitances are not degraded as would it be the case if the buried oxide was scaled in SOI. The back-gate-to-substrate capacitance only is increased in GAA, but it presents a smaller area than that of the total source/drain regions. The extension of the back portion of the gate below the source/drain regions (Figure 4.1) also yields increased overlap capacitances, which could be eliminated by proper process. However, in this case, the heat evacuation through source/drain regions no longer profits from the enhancement provided by the GAA structure.

2. Comparison with experimental data

The predicted reduction of the self-heating effects in GAA devices will now be submitted to experimental verification. Transient current as well as four-point gate resistance measurements will provide independent checks for the validity of the analytical analysis.

2.1. Four-point gate resistance measurements

The first experimental confirmation of the excellent heat evacuation in GAA devices has been obtained by means of four-point gate resistance measurements. This method has already been applied with success to regular SOI devices [3]. The top view of the experimental test structure is depicted in Figure 4.5. $L_g \cong$ 2.9µm is the effective gate length and L_T = 18µm is the total length separating the sensing pads. Both SOI and GAA structures have been realized on the same wafer.

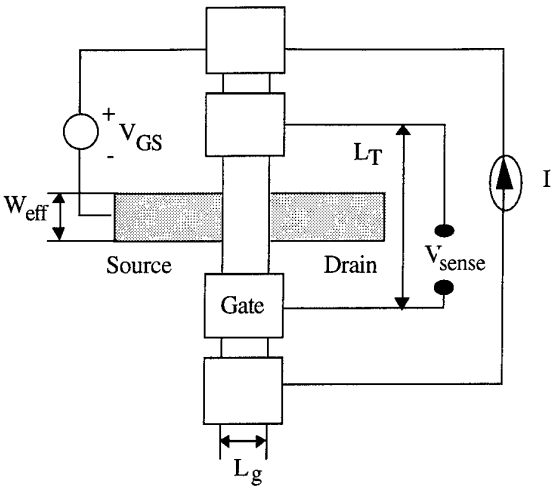

Figure 4.5: Top view of the experimental structure used for four-point gate resistance measurements.

The temperature dependence of the gate resistance R_G was first calibrated with the device turned off and homogeneously heated on a variable temperature chuck (the chuck already used for temperature measurements in Chapter III actually). Measurements, depicted in Figure 4.6, are obtained reproducibly in SOI as well as in GAA devices independently on the transistor type (n- or p-channel). The temperature sensitivity of the gate resistance $\xi = \Delta R_g/\Delta T$ is 0.18[Ω/°C] or equivalently $0.18 L_g/L_T[\Omega/\text{sqC}^\circ]$. On the contrary to what was previously observed [3], the gate resistance increases with temperature, due to the reduction of the carrier mobility in the N^+ polysilicon layer.

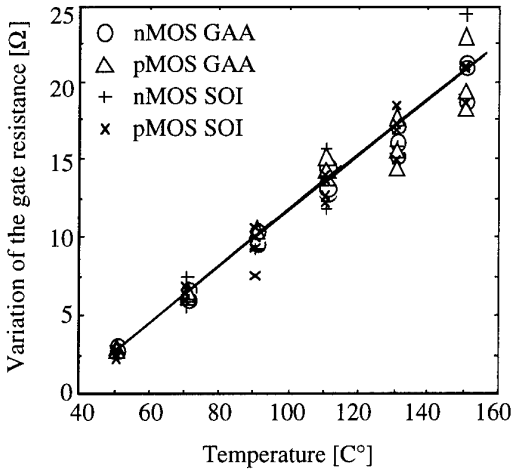

Figure 4.6: Variation of the N^+ polysilicon gate resistance with temperature, referenced to room-temperature.

In a second step, the resistance of the gate is recorded as a function of the power $P = [V_D - 2R_S I_D] I_D$ that flows through the device. R_S is the parasitic resistance of the source/drain regions. Results for n- as well as p-channel transistors are plotted in Figure 4.7. The variation of the gate resistance with temperature is not very large (because square devices were used) such that the measurement spread is non negligible especially at low power.

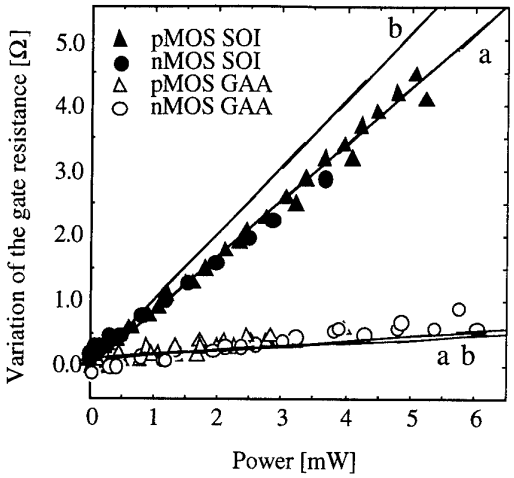

Figure 4.7: Experimental (dots) and analytically predicted (lines) variation of the gate resistance as a function of the dissipated power in 3μm × 3μm SOI and GAA devices. The model assumes a) $L_{eff} = W_{eff} = 3\mu m$ and b) $L_{eff} = W_{eff} = 2.5\mu m$.

The analytical model assumes a uniform heating of the gate just above or below the channel and an exponential temperature decay characterized by Λ_g outside the channel region. The total heated portion of the gate comprised between the sensing pads is therefore no longer L_T, as during the calibration procedure, but $W_{eff}+2\Lambda_g$. Taking this correction into account, the variation of the gate resistance ΔR_G is then simply proportional to the sensitivity ξ previously determined and to the temperature elevation of the gate. Finally, as a function of the dissipated power P, one obtains:

$$\Delta R_G = \xi_{\square} \frac{W_{eff} + 2\Lambda_g}{L_g} \Delta T_g = \xi \frac{W_{eff} + 2\Lambda_g}{L_T} \frac{G_{chf}}{G_{chf} + G_g} \frac{P}{G_T} \tag{4-3}$$

Straight lines in Figure 4.7 represent relationship (4-3) for both GAA and SOI cases. It is clear that the variation of the gate resistance is about an order of magnitude smaller in GAA than in SOI transistors due to the combined effects of higher global thermal conductivity G_T, lower temperature decay length Λ_g and smaller ratio of gate-to-channel temperature $\Delta T_g/\Delta T$. Figure 4.6 shows that relationship (4-3) is very sensitive to the device dimensions which are not necessarily accurately known. Assuming $L_{eff} = W_{eff} = 3\mu m$, the predicted slope $\Delta R_G/P$ nearly perfectly fits the measurements for SOI as well as for GAA devices (curves a). Nevertheless, with $L_{eff} = W_{eff} = 2.5\mu m$, that should better represent actual devices, the predictions overestimate the measurements in SOI (curves b). The reason could be that the model suffers from the uniform temperature approximation which is not accurate as soon as $L_{eff} > L_{s,d}$ (= 1.25μm). As far as the GAA structure is concerned, the reduction of the self-heating is obvious but this experimental method is not sensitive enough to draw reliable conclusions about the validity of the analytical model. Another independent technique will now be presented.

2.2. Transient drain current measurements: heating time constant

The second experimental method records the transient current that flows through the device when a step voltage is applied to the drain [2]. We consider n-channel MOSFETs.

The transient current is evaluated from the voltage drop across a load resistor connected to the source of the transistor as shown in Figure 4.8.

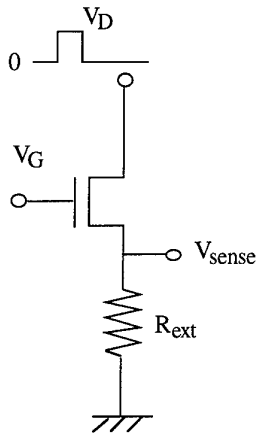

Figure 4.8: Measurement set-up for transient drain current analysis.

The external source resistance R_{ext} (100Ω & 56Ω) was chosen small enough such that the low-pass filter it forms with the input capacitance of the scope (RC ~ 10^{-9}s) does not interfere with the time constant associated with self-heating (τ ~ 10^{-6}s). GAA and SOI devices were operated with V_G = 6V and 8V respectively. Impact ionization is negligible as long as $V_D \leq V_G - V_{th}$. Rise/fall time, width and period of the drain pulse were 10ns, 10µs and 60µs respectively as proposed in [2].

Figure 4.9 compares semi logarithmic plots of the resulting drain current transient characteristics observed in both 3µm × 3µm regular SOI and GAA devices, with V_D = 5V and 7V respectively which corresponds to the same dissipated power $P = V'_D I_D \approx 4$ ... 4.5mW. The corrected drain voltage V'_D is given by $V_D - (2R_S + R_{ext})I_D$. The step-like shape of the curve is due to the quantization error of the scope. The voltage drop across R_{ext} is measured with an accuracy of 0.1mV (error of 1µA on the current). As expected, the current decrease, attributed to self-heating, is more pronounced and occurs with a longer time constant in SOI devices than in GAA transistors.

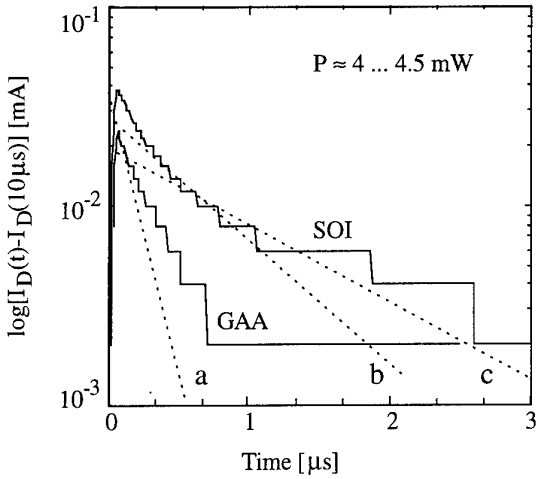

Figure 4.9: Transient drain current characteristics in 3µm × 3µm nMOS SOI and GAA devices. Dashed lines represent different time constants: a) 0.3µs, b) 1.6µs, c) 2.6µs.

The heating time constant τ can then be estimated as [2]:

$$\tau = \frac{\rho_{Si} c_{Si} V_{Si} + \rho_{SiO_2} c_{SiO_2} V_{SiO_2}}{G_T} \tag{4-4}$$

with ρ and c the densities and specific heats of the materials listed in Table 4.2. V_{Si} and V_{SiO_2} are the heated volumes of Si and SiO_2, respectively darkened and hatched in Figure 4.10. Still assuming that the top of the substrate is the thermal ground plane and that the temperature decays linearly in the buried oxide, V_{Si} and V_{SiO_2} in SOI devices can be approximated by:

$$V_{SiO_2} = \left(W_{eff}\left[L_{eff} + 2\Lambda_{s,d}\right] + 2\Lambda_g L_g\right)\left(t_{top} + \frac{t_{oxb}}{2}\right)$$

$$V_{Si} = W_{eff}\left(L_{eff} + 2\Lambda_{s,d}\right)t_{si} + L_g\left(W_{eff} + 2\Lambda_g\right)t_{gate}$$

with t_{top} = 1µm, the thickness of the covering top oxide layer. The expressions for GAA structures are:

$$V_{SiO_2} = \left(W_{eff}\left[L_{eff} + 2\Lambda_{s,d}\right] + 2\Lambda_g L_g\right)\left(t_{top} + t_{oxf}\right)$$

$$V_{Si} = W_{eff}\left(L_{eff} + 2\Lambda_{s,d}\right)\left(t_{si} + \frac{t_{backgate}}{2}\right) + L_g\left(W_{eff} + 2\Lambda_g\right)t_{gate}$$

Using (4-2) and (4-4) together with the values of W_{eff} and L_{eff} mentioned in Table 4.1, the following numerical results are obtained: $\tau_{GAA} \approx 0.3\mu s$ and $\tau_{SOI} \approx 2.6\mu s$. Dashed lines in Figure 4.8 indicate those time constants (curves a and c). The predicted τ_{GAA} and τ_{SOI} are respectively smaller than the prompt decay in GAA and slightly larger than the tail decay in SOI. Assuming that only one half of the top oxide layer is really heated in SOI brings τ_{SOI} down to 1.6µs (curve b) which fits the middle of the curve and shows the large importance of t_{top}. Discrepancies between model and experiments again arise from the uniform temperature assumption. On the other hand, τ is not strongly sensitive to the effective device dimensions. Hence, although W_{eff} is slightly smaller in GAA than in SOI transistors, the difference of device width cannot account for the strong decrease of the heating time constant. GAA devices reach quickly heat equilibrium ($\tau_{SOI}/\tau_{GAA} \approx 10$) owing to the larger global thermal conductance ($G_{T,GAA}/G_{T,SOI} \approx 3$) but also owing to the strong reduction of the heated volumes (the shrinking of the temperature decay lengths accounts for another factor 3).

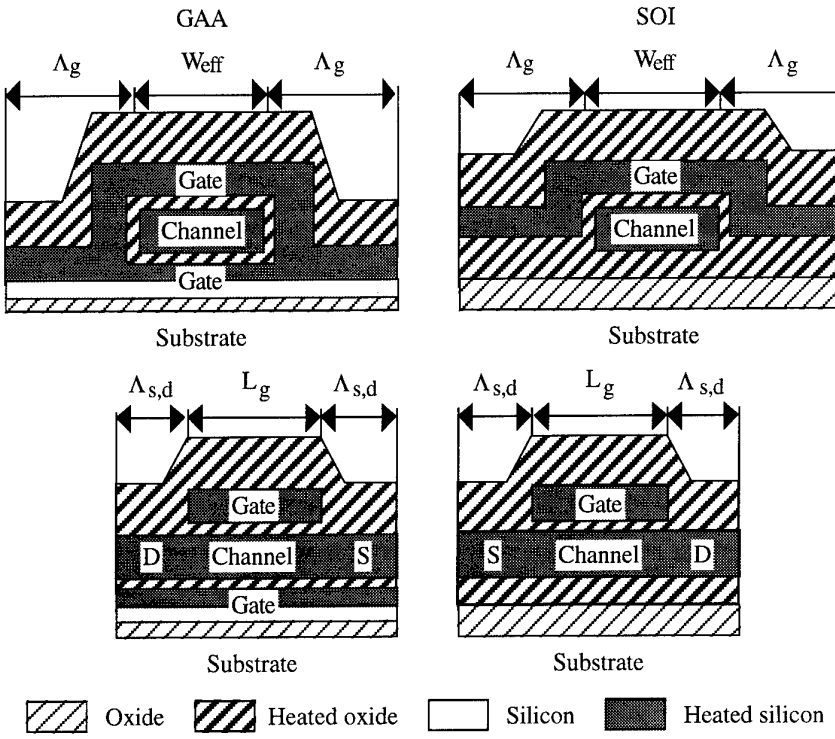

Figure 4.10: Heated silicon and silicon dioxide volumes in transversal (top) and longitudinal (bottom) cross-sections of GAA and SOI devices.

2.3. Transient drain current measurements: current reduction

A good correlation between predicted and measured current evolution due to self-heating can also be highlighted. Recording the peak and the steady-state level of the transient drain current for each value of V_D (swept between 0.5V and V_G), non-heated (solid circles) and heated (open circles) I_D-V_D characteristics can be plotted point by point in Figure 4.11. Analytical drain current characteristics, also added in Figure 4.11 (lines), were obtained according to the procedure described in [2] when including the self-heating or not. The temperature rise in the channel is computed iteratively with:

$$\Delta T = I_D(300+\Delta T)V'_D/G_T \qquad (4\text{-}5)$$

until convergence is obtained. The complete set of equations giving the current in linear and saturation regimes as well as the fitting parameters (such as the mobility and the threshold voltage at room temperature, and the parasitic resistances) are presented in the Annex. The same temperature variations are assumed in GAA and SOI devices for the mobility and the threshold voltage, which is rightful below 200°C, as experimentally observed (Figures 3.6 and 3.3). Figure 4.11 demonstrates that the set of parameters which nicely fits the initial curve (without self-heating), is still adequate when self-heating occurs. This clearly indicates that the computation of G_T used in (4-5) is valid for both SOI and GAA cases.

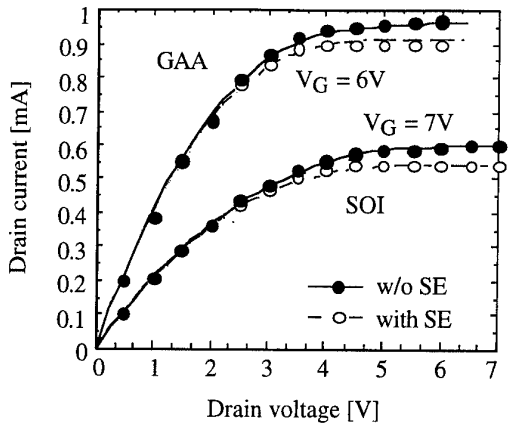

Figure 4.11: Experimental (circles) and analytical (lines) drain current curves as a function of the drain voltage with and without self-heating (SE) in 3µm × 3µm nMOS SOI and GAA devices.

The dots in Figure 4.12 presents $\Delta I_D/I_D$ the experimental variation of the drain current due to self-heating, normalized to the case where self-heating is absent, as a function of the dissipated power $P = I_D V'_D$. Best linear regressions show that $\Delta I_D/I_D$ follows P nearly linearly with a slope equal to 0.35[W^{-1}] in SOI devices and about half this value (*i.e.* 0.18[W^{-1}]) in GAA transistors. The consequence is that similar relative current reduction is expected in both GAA and SOI devices at same gate voltage overdrive, although the driving capability (and hence the power) of GAA devices is more than twice that of SOI transistors.

The relative current reductions analytically predicted by the iterative procedure (4-5) are plotted in Figure 4.12 as well. We have checked that this model is only slightly sensitive to R_S and is nearly independent of V_G. The analytical model better approximates the SOI than the GAA behavior especially in the saturation region (high power). Once more, the reason is that, in saturation, the power is mainly dissipated in the pinch-off region where there is a peak of electric field. The uniform temperature approximation is then badly appropriate in the GAA case where the channel length is about five times larger than the temperature decay lengths in source/drain regions.

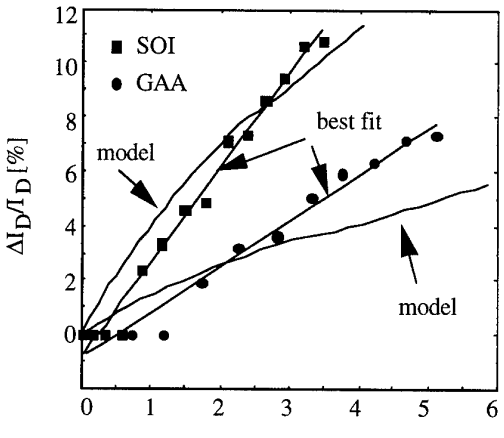

Figure 4.12: Experimental variation of the drain current (normalized to the case where self-heating is absent) (dots) and its best linear fit as a function of the dissipated power in 3µm × 3µm nMOS SOI and GAA devices. Results from the model are shown as well.

Finally, Figure 4.13 presents the channel temperature elevation obtained from (4-5) as a function of the dissipated power (symbols). 2D simulation results are also depicted (lines). The BC1-curve assumes no heat flow through the front gate. The BC2-curve is obtained with a more realistic boundary condition on top of the front gate and should be closer to 3D simulation results. Model and simulations are close together for P < 3mW. At larger power, 3D simulations are absolutely mandatory to get reliable conclusions. The model predicts that ΔT follows P linearly. The SOI slope exceeds the GAA slope by more than a factor of 2. At P ≈ 3mW, ΔT is around 30K in SOI and only around 10K in GAA.

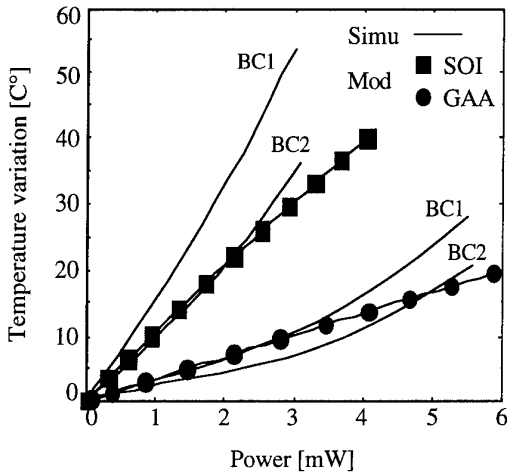

Figure 4.13: Predictions of channel temperature elevation obtained by the model (symbol) and 2D simulations (lines) as a function of dissipated power in 3μm × 3μm nMOS SOI and GAA devices. BC1 and BC2 refer to worst case and realistic boundary conditions on the top gate.

3. Conclusions

Self-heating problems are very annoying in power SOI devices. Following an approach similar to [2], an analytical model was used to clearly emphasize the advantage provided by the scaling of the buried oxide on the heat evacuation. The heat flow was shown to follow a $(t_{oxb})^{-n}$-law with 0.5 < n < 1, and strongly depends on the device dimensions. Three experimental independent evidences of reduced self-heating in GAA devices were provided and quantitatively justified by the analytical model. The advantage of the GAA structure is to replace the buried oxide below the channel by the back polysilicon gate, which benefits for a much larger thermal conductivity. To achieve the same result in SOI devices, the buried oxide thickness should be reduced down to twice the gate oxide thickness, which unfortunately would also lead to a dramatic increase of the source/drain and interconnection parasitic capacitances with the substrate. In GAA transistors, on the contrary, source/drain regions and interconnections still lie on the thick buried oxide layer so that those parasitic elements are kept small. We will now focus on the enhancement provided by the GAA technology in radiative environments.

Annex

The model used to calculate the drain current has already been applied with success to SOI devices [2]. First of all, the parasitic source/drain series resistances R_S and the externally added resistance R_{ext} must be incorporated in the calculations: the corrected drain voltage and gate bias are $V'_D = V_D-(2R_S+R_{ext})I_D$ and $V'_G = V_G-(R_S+R_{ext})I_D$ respectively. The model for the drain current in linear operation is:

$$I_D = \frac{W_{eff}}{L_{eff}} \frac{\mu}{1+V'_D/(E_{sat}L)} C_{ox}\left(V'_G - V_{th} - \frac{V'_D}{2}\right)V'_D$$

while, in the saturation region, the following expression is used:

$$I_D = \upsilon_{sat} W_{eff} C_{ox}\left(V'_G - V_{th} - V'_{Dsat}\right)$$

The saturation velocity υ_{sat} is assumed to be constant because of its negligible temperature dependence. The temperature dependence for the mobility μ and the threshold voltage V_{th} are respectively given by [2]:

$$\mu(T) = \mu_0\left(\frac{T}{300}\right)^{-1.76}$$

$$V_{th}(T) = V_{th0} - 1.35\times10^{-3}(T-300)$$

where μ_0 and V_{th0} are room-temperature values. From the results of Chapter III, it is licit, below 200°C, to adopt the same temperature variations in SOI and GAA transistors.

The lateral electric field at the edge of the velocity saturation region E_{sat} and the voltage drop across the non-saturation portion of the channel V'_{Dsat} are obtained by means of the following set of coupled equations solved iteratively:

$$E_{sat} = \frac{2\upsilon_{sat}}{\mu}$$

$$V'_{Dsat} = \frac{E_{sat}(L_{eff}-\Delta L)\left(V'_G - V_{th}\right)}{E_{sat}(L_{eff}-\Delta L)+\left(V'_G - V_{th}\right)}$$

$$V'_D = V'_{Dsat} + x\,E_{sat}\sinh\left(\frac{\Delta L}{x}\right)$$

with $x = 0.22t_{si}^{1/2}t_{oxf}^{1/3}$.

Calculations were performed with the saturation velocity υ_{sat} equal to 7.87×10^6[cm/s] and with the room-temperature value of the threshold voltage V_{th0} equal to 0.57[V] and 0.52[V] in nMOS SOI and GAA devices, respectively. The best fitting with the experimental initial drain current curve (T = 300K) has been obtained with $R_S = 510\Omega$; $\mu_0 = 370$[cm^2/(Vs)] in SOI devices and with $R_S = 110\Omega$; $\mu_0 = 2*475$[cm^2/(Vs)] in GAA transistors.

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Chapter V: GAA device in radiative environments

The three following chapters being dedicated to the various facets of radiation hardness techniques, it is first necessary to define and briefly introduce the main concepts, problems and challenges which the designer is facing when dealing with radiative environments. After this introductory part, Chapter V shows why the GAA structure is expected to provide the best hardening-by-technology approach in combining the advantages of both bulk devices (concerning total-dose hardness) and SOI transistors (as far as Single-Event-Upset (SEU) is concerned). Total-dose performance of isolated devices is then presented and confirms expectations.

Chapter VI investigates how far circuit design can improve the total-dose irradiation hardness of static memories (SRAMs) fabricated in a soft process such as FD SOI. It is shown that no optimum design can prevent memory operation failure when charge trapping in the buried oxide induces excessive leakage currents in n-channel devices. The total-dose hardness hence mainly relies on the choice of a proper technology and the GAA process is suspected to be the best candidate. To confirm this point, the excellent characteristics up to 85Mrad(Si) irradiation of a standard designed 1k GAA SRAM are presented.

Finally, Chapter VII deals with the SEU hardness of SRAMs. Here again, the double-gate structure dramatically improves the performance of regular SOI devices. Slow charge collection process and quite large parasitic resistances and capacitances are responsible for the GAA success. A new temporal model for SEU is also developed since the existing static analysis is insufficient to fully justify the excellent GAA results.

1. Introduction

Many applications require integrated circuits tolerant to radiative environments, such as nuclear reactors, nuclear weapons, large accelerators and satellites or space shuttles. A large variety of particles with energies ranging from keV to GeV can be found in these environments [1,2,3]:

- in nuclear plants, robotic electronics is essentially submitted to γ-irradiation and/or to high neutron fluxes.
- high-dose-rate weapons are susceptible to generate X-rays and γ-rays essentially.

- high-energy research is carried out on beams of electrons and protons that collide to produce inside the detecting electronics very energetic protons, kaons, photons, neutrons, electrons, and mostly charged and neutral pions.
- the natural space environment contains high-energy protons and electrons, trapped by the earth's magnetic field, as well as cosmic rays (protons, alpha particles and heavy ions), coming from the sun and the galactic system. The fluxes and type of particles vary significantly with altitude and angle of inclination.

Fortunately these various energetic particles generate a restricted number of electrical effects in microelectronic devices and can be characterized by few well-chosen parameters.

1.1. Interaction of radiations with microelectronic devices [4,5]

The interactions of incoming particles with microelectronic devices can be divided into two mechanisms: ionizing and non-ionizing energy losses, occurring respectively for photons, electrons, protons, energetic heavy ions on one hand, and high-energy particles (protons, neutrons) on the other hand.

In non-ionizing energy losses, the energy transferred to the atom is so high that the atom is knocked free from its lattice site, leaving a vacancy behind. The displaced atom can in turn collide and displace another atom. This process repeats until the energy transferred is high enough to displace a neighboring atom and produces a "cascade" of displacements. These defects can act as generation or recombination centers and modify the lifetime of minority carriers which is essentially critical for bipolar technologies.

In ionizing energy losses, the incident particle interacts with peripheral electrons of atoms and create free electron-hole pairs that in turn can generate additional pairs. The energy required to produce one electron-hole pair $E_{e-/p+}$ is related to the bandgap energy of the semiconductor E_g by the following empirical relationship: $E_{e-/p+}(eV) = 2.67E_g$ (eV) +0.87. It appears that, whatever the type of radiation, the energy deposited is the only parameter necessary to describe the phenomenon. By definition, the absorbed dose D is the energy deposited per unit of mass. The MKS unit for dose is the gray (Gy) which corresponds to the deposition of 1 joule of radiation energy per kilogram of matter. An old unit, still commonly used, is the rad(Si) which is defined by the deposition of 100 erg of radiation energy per gram of silicon. The equivalence between the two units is straightforward: 1 Gy = 100 rad. The number of electron-hole pairs dN which are generated by the deposition of the energy dE in the volume dV of the material is related to the dose by [6]:

$$\frac{dN}{dV} = \frac{1}{E_{e^-/p^+}} \frac{dE}{dV} = \frac{\rho}{E_{e^-/p^+}} D \qquad (5\text{-}1)$$

where ρ is the density of the material. It is generally admitted that 1 rad generates $4x10^{13}$ pairs per cm^3 in silicon ($E_{e-/p+}$ = 3.6 eV) and $7.6x10^{12}$ pairs per cm^3 in SiO_2. This free carrier generation is a concern for both insulator and silicon: the generated carriers induce permanent effects in insulator, and transient currents in silicon.

1.2. Permanent effects - Total-dose [4,5]

1.2.1. Mechanisms [7]

Some electron-hole pairs that are generated uniformly throughout an oxide layer undergo, just after creation, columnar and/or geminate recombination. The escaping electrons will rapidly drift out of the oxide (within picoseconds) while holes, about 10^6 times less mobile than electrons, slowly drift toward one interface depending on the electric field direction. A fraction α of the hole reaching the Si/SiO_2 interface is trapped in pre-existing neutral hole traps, creating a positive "permanent" charge Q_{ox} (C/cm^2) [8]. α being related to the number of neutral traps that exist at the Si/SiO_2 interface, is strongly dependent on the technology: typical values are 0.3 for normal, unhardened oxides and 0.05 or less for rad-hard oxides. The oxide trapped charge Q_{ox} is susceptible to anneal either if trapped holes are thermally emitted to the valence band of silicon or if electrons in the conduction band of silicon join the trapped holes by tunneling through the oxide. Annealing is therefore activated by applying a positive field and by increasing the temperature.

In addition to the trapping of holes, a build-up of "interface traps" also occurs upon radiation exposure. At the Si/SiO_2 interface, the natural mismatch of the physical network creates uncompleted chemical bonds which are electrically active. They form energy states in the silicon bandgap which can capture the carriers present in silicon just below the interface. As a consequence, a fundamental property (called amphoteric behavior) of these interface states is that the net charge residing in them can either be positive, (neutral) or negative [9,10]. The charge is positive when the surface layer is made of holes. This case is obtained when the Fermi level at the interface is below the neutral Fermi level (Fermi level in the substrate of the equivalent bulk device, which is somewhere near the midgap position). The net charge is negative when the Fermi level at the interface is above the neutral Fermi level (surface electron layer).

The amount of interface traps increases under irradiation exposure following a mechanism not yet fully understood. The key point is that, during the fabrication process, hydrogen is incorporated in the (gate) oxide network as -OH groups which easily break. Excitations within the oxide caused by irradiation such as the hopping drift of holes, tend to disrupt these -OH bonds, creating new dangling bonds at the interface [11,12]. The annealing of trapped holes can also create additional interface traps. Creation of interface states is therefore generally delayed. It is quite clear that interface states usually do not anneal out with time.

A schematic representation of the basic mechanisms described above and their position relatively to the Si/SiO_2 interface is given in Figure 5.1 after [13].

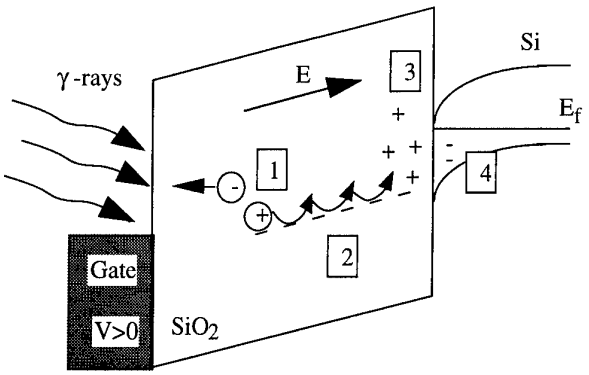

Figure 5.1: Illustration of the main processes for radiation-induced charge generation in a n-channel MOSFETs with a positive gate bias [13]:
1) electron-hole pairs generation and separation; 2) hopping transport of holes through localized states; 3) deep hole trapping near the Si/SiO_2 interface; 4) interface traps build-up.

1.2.2. Electrical influences

In MOS devices, the positive charge Q_{ox} decreases the threshold voltage of both n- and p-channel transistors. Assuming that Q_{ox} is proportional to the oxide thickness t_{ox}, the threshold voltage shift ΔV_{th} is proportional to t_{ox}^2 [6,10]:

$$\Delta V_{th} = \frac{-Q_{ox}t_{ox}}{\varepsilon_{ox}} = -\alpha\frac{q\rho}{\varepsilon_{ox}E_{e^-/p^+}}t_{ox}^2 D \qquad (5\text{-}2)$$

A thickness-cubed dependence results if, in addition, the characteristic penetration depth of the traps into the SiO_2 is proportional to the oxide thickness [14,15]. Reducing the thickness of the oxide layers in contact with the active silicon region is therefore a key point to achieve a radiation-hard technology.

The trapped-charge-induced effects are highly dependent on the gate bias applied to the device during irradiation. Worst-case conditions correspond to positive gate biases. In this case indeed, holes all drift toward the Si/SiO_2 interface where they have a non-zero probability of becoming trapped. On the contrary, for negative gate bias, holes drift toward the gate electrode and only those created in the small region close to the Si/SiO_2 interface have a non-zero probability of becoming trapped near this interface. The space-charge build-up saturates with increasing dose because it cancels the effect of the applied voltage: the space-charge region grows until most of the voltage applied to the insulator appears across it, bringing the electric field elsewhere in the insulator to a small fraction of its original value [16].

Due to their amphoteric behavior, interface states capture hole in p-channel devices and electrons in n-type transistors. As a result, they decrease the p-type threshold voltage, but they contribute negatively to the charge in n-channel devices and tend to offset the positive charge from trapped holes. Since the hole trapping tends to saturate with dose while the interface state build-up does not, the overall negative flat-band or threshold voltage shift tends to slow down and then to reverse in n-type transistors. This phenomenon called "rebound" could occur during irradiation if the interface trap

generation is sufficiently large as illustrated in Figure 5.2 by curve a. The rebound is highly dependent on the technology, and the lower the dose-rate, the lower the dose at which it appears [17]. Whatever the technology, a rebound occurs when irradiation has stopped, as depicted in Figure 5.2 by curve b, since Q_{ox} anneal out with time (phenomenon activated by increasing the temperature) while the number of interface states is stable or even continues to grow.

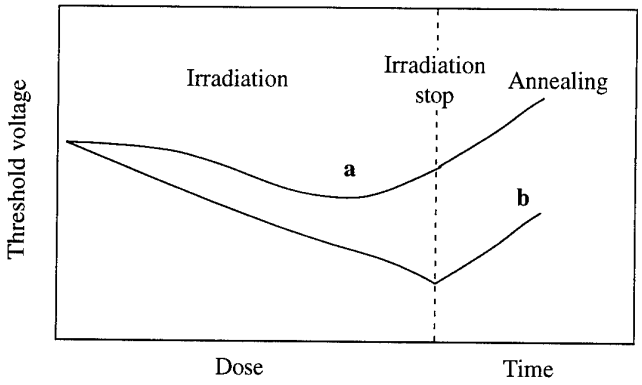

Figure 5.2: "Rebound" effect in the n-channel MOSFET threshold voltage:
(a) Large interface state generation inducing rebound during irradiation,
(b) Small interface state generation during irradiation and rebound after irradiation stop.

Interface states also induce an increase of the carrier surface recombination velocity.

1.2.3. Requirements of actual applications

Table 5.1 gives an idea of the magnitude of total-dose irradiation levels to which devices can be submitted: during their lifetime, satellites orbiting around the earth receive total-doses ranging between 10krad(Si) and 1Mrad(Si), depending on the orbit parameters [18]. Interplanetary spacecrafts and some electronics used to dismantle nuclear reactors can be exposed to doses in excess of 10Mrad(Si). In the same range, a cumulated dose of 1 to 10Mrad(Si)/year is expected in the internal detectors of the future Large Hadron Collider at CERN [19]. Some hot cells or lifting units dedicated to the reprocessing of nuclear waste should survive to 100Mrad(Si) accumulated during their short lifetime (around 5 years) [20]. Finally, even more challenging is the monitoring and/or maintenance of fission and fusion reactors that require a total-dose hardness of 1Grad(Si) and 30Grad(Si) respectively [21].

The term "total-dose" supposes that all the defects induced by irradiation are time-stable and only depends on the absorbed dose. It has been explained that these assumptions are generally not verified in MOS ICs where many other variables such as time, energy of particles, sign and amplitude of the applied electric fields, temperature, ... and, last but not least, dose-rate, are susceptible to strongly modify the results. The problem is that laboratory tests are performed with X-ray or ^{60}Co-γ sources with a typical dose-rate of 3-10^3rad(Si)/s delivered during 10^0-10^5 seconds, while actual applications involve other particles and totally different dose-rates (Table 5.1): nuclear weapons typically produce flashes at high dose-rate (10^9rad(Si)/s) during 10^{-9}...10^{-3}s while the natural space provides a continuous low dose-rate (0.05-0.2rad(Si)/s) irradiation [2]. As a

consequence, it is not obvious to define standard laboratory tests and worst-case operating conditions. Nevertheless, provided that some corrections and adjustments are made, the ^{60}Co irradiation furnishes a reasonable simulation of low-dose-rate space and high-energy collide applications, while it is especially suitable to test components that should survive in nuclear reactor environments. Clearly, making connection between laboratory tests and possible real use is a very difficult challenge, beyond the scope of this study. Since each experiment is well documented about the tests conditions and about the procedure used to measure and extract the electrical parameters, comparison with previously published studies is however possible.

Table 5.1: Typical radiation-hard applications and their parameters.

Application	Dose-rate rad(Si)/s	Total-dose rad(Si)
Space		
orbiting satellite	0.05 - 0.2	10^4 - 10^6
interplanetary spacecraft	0.05 - 0.2	10^7 - ...
High energy physics		
LHC - CERN		10^6 - 10^7
Nuclear field		
decontamination	0.03 - 0.3	10^3 - 10^5
reactor dismantling	0.3 - 3	10^4 - 10^6
waste reprocessing	0.3 - 30	10^5 - 10^8
fission reactor monitoring	0.03 - 3×10^3	10^5 - 10^9
fusion reactor maintenance	3×10^2 - 3×10^3	10^9 - 3×10^{10}
Nuclear weapons	10^9	

1.3. Transient effects

1.3.1. Mechanisms [4]

When alpha particles or heavy ions (cosmic rays) penetrate into silicon, they create, along their path, a very high density plasma of electron-hole pairs. Protons also induce a very dense plasma but not by direct ionization: they induce nuclear reaction in silicon and the recoiling fragments act as secondary ions, producing a plasma. If the energetic particle passes through a reverse-biased junction, the high concentrations of electrons and holes in the plasma will distort the original depletion region into a cylinder which follows the path of the particle. As a consequence, the junction field creates a "funnel" region that extends down into the underlying substrate as depicted in Figure 5.3 (left part). The electric field within the junction depletion region and the funnel region will cause the carriers to be separated and rapidly collected by the sensitive electrode and the back electrode following a drift mechanism. This charge collection creates a parasitic photocurrent. In bulk silicon devices, the amount of charge that is collected by drift is

greatly enhanced by the funnel action since the funnel extends typically on the order of ten micrometers. The drift of carriers to the electrodes occurs within hundred of picoseconds after the particle strike. Diffusion of carriers to the edge of the funnel region constitutes another component to the collected charge. But the diffusion of carriers takes much longer than the drift component, up to hundred of nanoseconds.

The amount of energy that a particle deposits per unit depth in a material is given by its stopping power. The mass-stopping power is defined as the Linear Energy Transfer (LET) and is given by:

$$LET = \frac{1}{\rho}\frac{dE}{dx} \tag{5-3}$$

where x is the linear distance along the particle track, dE/dx is the rate of energy loss in the material, and ρ is the density of the material. The LET is usually expressed in MeV•cm^2/mg. For a given particle, the LET depends on the material and the energy, and can be either calculated using specialized codes (TRIM code [22]) or found in Tables (Northcliffe and Scilling [23], Ziegler [24]). The important parameter is the charge deposited in the particle track obtained, in the units of pC/µm, from the relationship:

$$Q = \frac{1.6\times10^{-2}\cdot LET\cdot\rho}{E_{e^-/p^+}} \tag{5-4}$$

where $E_{e-/p+}$ is in units of eV, LET is in units of MeV•cm^2/mg and ρ is in units of g/cm^3. For an LET of 50MeV•cm^2/mg, the charge deposited is approximately 0.5pC/µm in silicon.

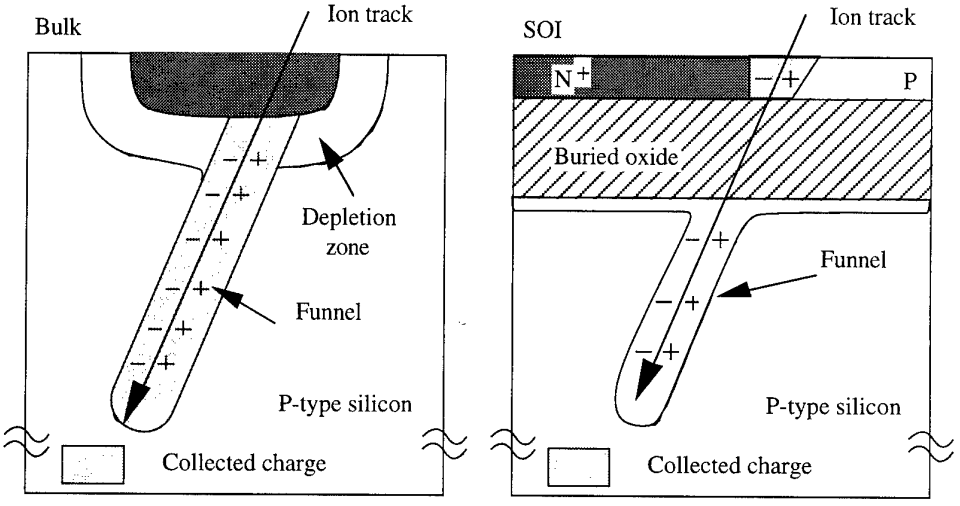

Figure 5.3: Ion strike and subsequent funneling effect in a reverse-biased bulk and SOI junction from [18].

1.3.2. Electrical effects [3,4]

The photocurrent collected by a sensitive electrode after a particle strike may induce two types of electrical failures:

• Soft failures

Photocurrents can change the state of a logic node and cause false information to be stored or propagated. This type of failure is known as Single-Event-Upset (SEU) and is a non-destructive or "soft" error. The most sensitive devices are DRAMs, SRAMs and microprocessors. In SRAMs, the memory cell flips into the complementary logical state if the voltage transient on the internal capacitance exceeds the noise margin. In DRAMs, the photocurrent discharges the storage capacitor, directly erasing the information. In a clocked circuit, the photocurrent acts as a noise spike that may propagate and modify the running program. A soft error can be corrected by reprogramming the circuit or restarting the algorithm. The Single-Event-Upset sensitivity is generally represented by a plot of the cross-section (which represents the equivalent sensitive area of the circuit) as a function of the LET of the incident particle. The smaller the cross-section, the less sensitive the devices are to SEU.

• Hard failures

Another class of Single-Event-Effects (SEE) termed "hard" errors, are not correctable. They include the Single-Event-Latchup (SEL), the Single-Event-Burnout (SEB) and the Single-Event-Gate-Rupture (SEGR). The SEL is observed in bulk CMOS technologies and consists in the triggering by photocurrents of parasitic thyristor structures which are then latched in the "on" state until the power supply to the circuit is interrupted. The SEB occurs when the device is destroyed by thermal dissipation, the latched current being only limited by low serial resistances of the conducting bipolar transistors. Finally, hard errors also include the SEGR obtained when the injected charge increases the electrical field across the oxide between gate and drain, inducing electrical breakdown.

2. The GAA structure as the best radiation-hardened-by-technology device

After discussing the advantages and drawbacks of bulk and SOI technologies to face total-dose and transient radiation effects, the GAA structure is proved to be the best hardened-by-technology candidate in the context of state-of-the-art CMOS processes.

2.1. The bulk CMOS technology

Bulk technologies offer a wide range of total-dose hardness capabilities. Standard (non-hardened) CMOS circuits can only sustain 10krad(Si) although levels of 100krad(Si) are sometimes reached but not guarantied [25]. Commercially available rad-hard CMOS products offer hardness assurance up to 1Mrad(Si) or beyond for some specific parts [25]. Experimental hardened CMOS circuits have been tested at levels of 50-100Mrad(Si) [26]. Therefore, the total-dose hardness of some bulk components could be sufficient for most applications, but bulk technologies encounter a serious problem as far as transient effects are concerned. Indeed, the evolution towards smaller device geometry and low-power operation reduces the critical charge required to induce Single-Event-Effects. As a consequence, SEU, SEL, SEB and SEGR will perhaps become more likely in the future. The use of SOI substrates offsets many of these transient effects.

2.2. The SOI CMOS technology [18,27]

In SOI devices, the absence of conducting path underneath the SOI MOS transistors completely eliminates parasitic pnpn paths that can cause SEL and SEB. Another huge advantage of SOI is the reduced sensitivity to SEU. Indeed, because of the presence of a buried insulator layer between the active silicon film and the substrate, none of the charges generated within the substrate by the particle strike can be collected by the junctions of the SOI devices (Figure 5.3, right part). The few collected electrons are those produced within the thin silicon film, the thickness of which is typically 150-300nm in radiation-hard applications (PD SOI). The ratio of the track lengths along which electrons can be collected gives a first-order approximation of the advantages of SOI over bulk: between the typical 10µm-track in the bulk substrate and the 200nm-thick SOI film, a factor ...50... is easily obtained. Nevertheless, in floating SOI films, the parasitic lateral bipolar structure is known to strongly amplify the injected charge so that the gain over bulk counterparts could be more reduced than expected from the above simple calculation [28,29]. Indeed, in floating body (n-channel) SOI devices, the hole current cannot escape by the substrate electrode, is therefore collected by the source junction, and serves as base current for the parasitic lateral npn transistor. Any bipolar action, even with a gain lower than unity, will therefore contribute to increase the collected current. The situation is of course worst in short channel devices where the bipolar gain is higher. Solutions include the use of body ties which unfortunately reduces compactness and carrier lifetime. Also, if the back-gate bias is such that the substrate under the buried oxide is depleted, SOI devices are not totally insensitive to funneling in the substrate [30]. Indeed, electrons generated along the particle track in the substrate drift and accumulated under the buried oxide where they are minority carriers with a long lifetime. These electrons immediately induce a positive mirror charge in the upper silicon. Electrons are then injected by the external circuit to restore equilibrium, which induces a current spike. This effect is not observed with the substrate underneath the buried oxide in inversion or accumulation because, in this case, majority carriers with very short lifetime are available for immediate recombination.

In despite of their strong inherent SEU hardness, SOI ICs unfortunately can be more sensitive to total-dose ionizing radiations than bulk ICs due to the many contacts of the active silicon region with thick oxide layers at sidewalls and at the back interface [31,32,33,34,35,36].

Classical lateral isolation of SOI devices (by LOCOS or oxidized mesa [37]) is inherently soft, since it comprises a rather thick oxide which is of lesser quality than the gate oxide. Although there is usually no edge leakage problem in p-channel devices, n-channel transistors can be seriously affected by parasitic edge transistor turn-on (Figure 5.6). Solutions include the optimization of the field oxide growth and higher sidewall doping. Nevertheless, the latter edge leakage suppression technique is poorly effective since most of the implanted boron segregates into the field oxide during its formation. Therefore, specially modified-designed transistors have to be used such as edgeless devices [36,38] (Figure 5.4a), H-gate MOSFETs with P^+ body contacts [39] (Figure 5.4b), n-channel devices with P^+ diffusion interrupt leakage paths between the N^+ source

and drain diffusions [40], devices with sidewall and back polysilicon layers [41,42,26] (Figure 5.4c) or devices with spatial separation of the top-gate and sidewall regions [43]. All these types of structures, however, consume significantly more silicon real estate than regular MOSFETs, and/or add complex processing steps.

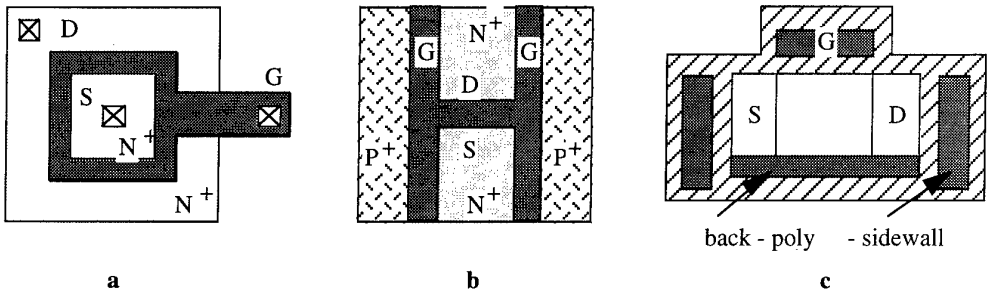

Figure 5.4: Different protection layouts against the lateral leakage in SOI MOS transistors:
(a) Ring-type or edgeless devices, (b) H-gate MOSFETs,
(c) Device with back and sidewall polysilicon layers.

N-channel SOI devices also require specific techniques to avoid back leakage that consists in the formation of an inversion layer at the back Si/SiO_2 interface [31]. By applying a negative back-gate bias during irradiation, holes generated in the buried oxide will preferentially drift toward the substrate electrode, reducing the charge accumulated near the interface with the active silicon. However, negative back-gate bias may jeopardize operation of p-channel devices. In partially-depleted devices, a peak of boron doping at the back interface is sometimes created to increase the threshold voltage of the back transistor. Non-fully depleted SOI circuits made in a 150nm-thick silicon film using this technique, have been reported to withstand doses up to 300Mrad(Si) [40]. However, non-fully depleted operation increases floating body effects and is detrimental to high temperature operation (Chapter III).

FD devices, despite their excellent electrical performance, are very bad candidates as far as total-dose hardness is concerned. First of all, they are usually too thin to allow the realization of a deep boron implant to suppress back leakage. Furthermore, even assuming that no back leakage occurs (which means that the back interface is either in depletion or in accumulation but not in inversion), FD devices are still sensitive to the charge accumulated at the back interface. Indeed, with the back interface in depletion, front and back gates are electrically coupled and both the subthreshold slope and the threshold voltage of the front transistor will degrade faster because of the exposed buried oxide. On the contrary, if the back interface is held in accumulation, the front threshold voltage shift with dose will be no worse than in a bulk transistor but the pre- (and hence post-radiation) subthreshold slope and transconductance will be poorer than in the equivalent bulk device [44].

Obviously the bulk process provides sufficient total-dose hardness but fails as far as SEU is concerned. On the other hand, the SOI process, inherently SEU-resistant, cannot offer a good total-dose hardness without sacrificing the ideal electrical performance of FD devices. A radical solution consists in using GAA devices.

2.3. The GAA technology

Since, their volume of active silicon is very thin and totally isolated from the substrate and from neighboring transistors, as in SOI devices, GAA transistors also benefit from latchup (SEL and SEB) immunity and from reduced SEU sensitivity. GAA devices should also be less susceptible to back funneling than SOI transistors since the top of the substrate is maintained in inversion by the action of the back-gate. Furthermore, if charges accumulate beneath the buried oxide, they will induce mirrored charges in the back-gate rather than in the top silicon layer.

On the other hand, unlike in regular SOI MOSFETs, the silicon film is neither in contact with the field oxide nor with the buried oxide so that the only radiation-generated charges that will influence the device electrical characteristics are found in the very thin, high-quality gate oxide. The shift of the device parameters upon radiation exposure is therefore very small.

As a result, GAA devices are expected to combine the strong SEL-SEU hardness of the SOI technology and the strong total-dose hardness of bulk circuits.

3. Total-dose hardness of the GAA structure

Provided that the thin, thermally grown gate insulator satisfies some basic requirements, the total-dose radiation hardness of the surrounding gate structure should be excellent and easily controllable. The fabrication process will be scanned in order to highlight the steps which are critical to obtain a high quality gate oxide. Experimental results will then illustrate the strong inherent total-dose hardness of the GAA structure over a wide range of gate bias conditions. The impact of the particular edge geometry of the device is also carefully examined.

3.1. Process hardening

To be radiation resistant, the gate insulator should at least satisfy three basic requirements: minimum charge accumulation, minimum interface state generation and the capability of operation under sufficiently high electric field intensities. Although companies successfully producing radiation-hard chips try to keep their processes as secret as possible, several guidelines can be found in the literature [45,46,47].

- Material: there is a general agreement that the best insulator is silicon dioxide.
- Thickness: charge accumulation is reduced by using an oxide as thin as possible since Q_{ox} is at least proportional to t_{ox} (inducing a threshold voltage shift proportional to t_{ox}^2). Nevertheless, too thin gate dielectrics cannot withstand sufficiently high gate voltages. The most favorable thickness is in the range 25-40nm.
- Process: last but not least, both α, the hole trapping factor of the oxide, and the number of interface traps should be minimized. This implies not only to form a gate oxide with a low content of contaminants and with an abrupt Si/SiO_2 interface, but also to maintain this high quality up to the completion of the process. First of all,

composition and temperature of the oxidizing ambient are decisive factors and published results are sometimes contradictory. In a steam ambient, the hardening is usually optimum at a lower temperature than commonly adopted in commercial processes (around 850°C) while growing the gate oxide in dry oxygen leads to the opposite conclusion [48]. The presence of chlorine (used to reduce metallic impurities) usually degrades the oxide hardness, although some recent experiments tend to demonstrate the contrary. Secondly, the post-oxidation annealing in nitrogen or argon also strongly influences the hardness. High temperature anneal appears to almost always degrade the performance. Finally, high temperature steps as well as ion implantation and soft X-ray irradiation through the gate oxide should be avoided up to the end of the process.
Since minimizing the quantity of hole traps is difficult, a new potential method proposes to introduce electron traps within the oxide. As a consequence, both electrons and holes would stay in the oxide and the total net charge could theoretically tends to zero. This last technique is, however, still on the drawing board and practical techniques for inducing electron trapping are yet to be found.

Our aim was not to develop a specially hard process, but, on the contrary, to show that the GAA structure is inherently robust even when realized without special care. Therefore, several of the overmentioned general rules have been adopted, but not all of them.

- The initial thinning of the silicon layer is performed by successive oxidation and oxide strip steps, which smooth the silicon surface (future Si/SiO_2 interface) and reduce the variability of the threshold voltage shifts subsequent to irradiation.
- Assuming that the gate oxide thickness to reach is 30nm, an initial gate oxide layer of 27nm is grown in a dry oxygen ambient at 950°C. Then low dose (10^{-11}...5×10^{-12} cm^{-2}) boron threshold voltage implants are carried out through the oxide which is therefore damaged but will not be removed. Indeed, regrowing a new gate oxide would cause all the implanted boron to segregate into this oxide. A small additional oxidation step is then performed to obtain the final thickness of 30nm. Annealing is carried out in an argon ambient with the temperature gradually decreased from 950° to 800°C.
- The temperature budget of all subsequent steps is minimized: the temperature of the phosphorus predoping of the polysilicon gate, ranges between 825°C and 900°C, and the source/drain annealing is performed at 850°C.
- Sputtered metallization, which is known to generate soft X-rays, was used (while not recommended) because it allows the deposition of an aluminum/silicon alloy which minimizes dissolution of source/drain silicon into metal. The radiation hardness of devices operating under negative gate-to-source bias should be most affected because the sputtering causes defects primarily in the upper part of the gate oxide layer near the top polysilicon gate.
- Finally, the post-metallization sintering (430°C during 30min in forming gas (nitrogen and hydrogen)), that is primarily intended to improve the metal-silicon contact, is also expected to reduce the pre-irradiation surface state density (and also the

number of radiation-induced surface states) although the presence of hydrogen is generally not beneficial to radiation hardness.

3.2. Experimental results

Clearly the process could be further improved to produce a gate oxide of better quality but this is not necessary. Indeed, it will be shown that the excellent GAA total-dose hardness mainly relies on the device geometry rather on the process: by simply decreasing the gate oxide thickness from 50nm to 30nm, the radiation hardness changes from very bad (lower than 100krad(Si)), to very good (higher than 85Mrad(Si)).

3.2.1. Soft process

The performance of GAA devices fabricated with a gate oxide thickness of 50nm and no additional boron implantation to avoid edge leakage is first discussed. Figure 5.5 (left) presents experimental drain current *vs.* gate voltage curves of 3μm × 3μm n-channel devices measured in linear operation (V_{DS} = 50mV) with dose as parameter. The corresponding evolution of the threshold voltage as a function of dose is also depicted in Figure 5.5 (right). The devices were measured *in situ* using an HP4145 semiconductor parameter analyzer and 5-meter long coaxial cables passing through the ^{60}Co irradiation chamber walls. All measurements could therefore be carried out without interrupting the irradiation process. The gate was held at 3V during irradiation, with all other terminals grounded. The threshold voltage drops from about 1V down to -0.7V after only 600krad(Si) irradiation, due to oxide charge build-up, and then slightly rebounds to -0.5V after 1Mrad(Si) irradiation owing to the influence of interface traps generation.

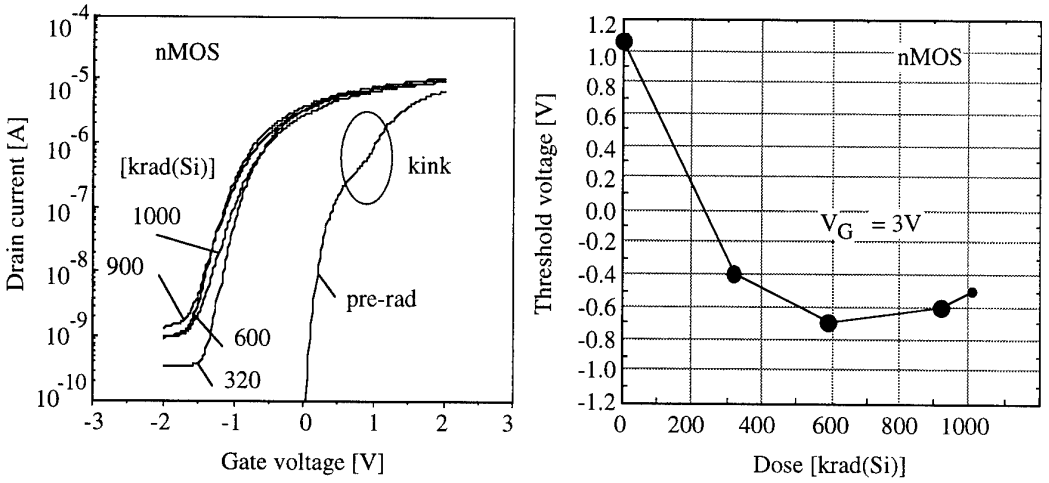

Figure 5.5: On the left, drain current *vs.* gate voltage curves of a 3μm × 3μm nMOS/GAA device exposed to different irradiation doses and, on the right, the corresponding threshold voltage *vs.* dose. V_G = 3V during ^{60}Co irradiation, and V_{DS} = 0.05V during parameter extraction.

3.2.2. The edge transistor

Although very bad as far as total-dose hardness is concerned, these results highlight an interesting phenomenon. The hump observed in the pre-rad logarithmic plot of the

drain current (Figure 5.5) is explained by the lower threshold voltage at the edges of the device due to the charge sharing between "front/back" and "lateral" gates [49]. Strangely enough, the edge leakage seems to disappear when the device is irradiated: in Figure 5.5, none of the curves measured after irradiation presents a kink.

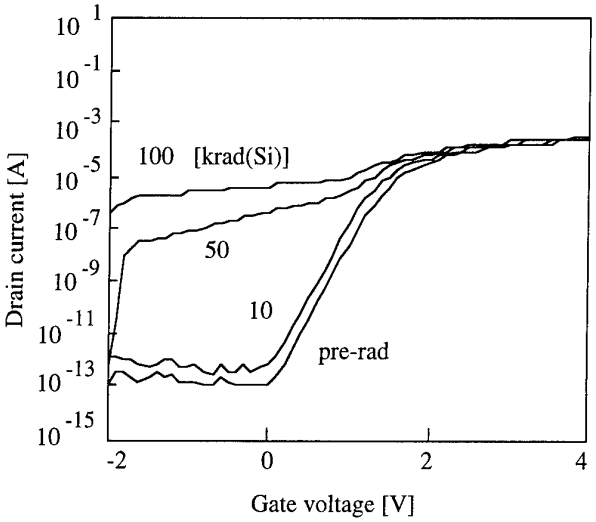

Figure 5.6: Drain current *vs.* gate voltage curves of a regular 20µm × 1.4µm LOCOS-isolated n-channel SOI device exposed to different irradiation doses from [38].
The 25nm-thick gate oxide was grown at 850°C. V_G = 5V; V_{DS} = V_{BS} = 0V during irradiation, and V_{DS} = 0.5V; V_{BS} = 0V during parameter extraction.

This GAA device behavior is opposite to what happens in LOCOS-isolated SOI MOSFETs (Figure 5.6) where the threshold voltage of the edge transistor shifts more upon irradiation than the main device threshold, thereby generating a permanent important subthreshold leakage [38].

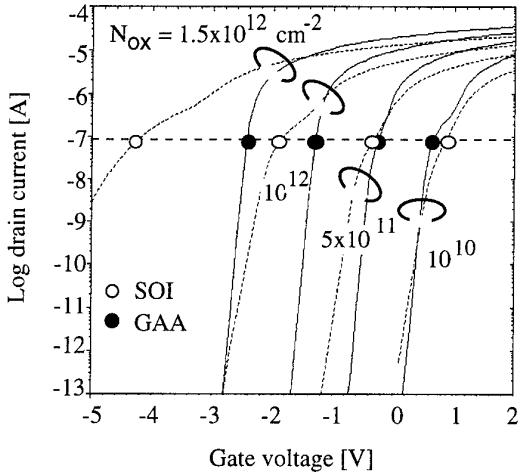

Figure 5.7: Simulated I_D-V_G curves of 3µm × 3µm n-channel GAA device (black circles) and SOI MOSFET (open circles) with different oxide charge densities. t_{oxf} = 50nm, t_{si} = 80(160)nm, t_{oxb} = 400nm, t_{oxe} = 50(200)nm in GAA(SOI). Uniform doping concentration.

Three-dimensional device simulations, published in Reference [50], are reported in Figure 5.7 and confirm that, with an increasing oxide charge density, the subthreshold

leakage disappears in GAA devices (black circles) and becomes worst (open circles) in SOI.

The structure used for simulations is an ideal mesa "corner" depicted in Figure 5.8. Two different thicknesses of the lateral oxide t_{oxe} are compared to simulate both SOI and GAA cases. The charge densities at the Si/SiO_2 interfaces have been uniformly increased to represent arbitrary irradiation doses. Simulations are therefore realistic for GAA devices, but they give best-case response of SOI transistors were buried and sidewall oxides, thicker and of lesser quality than the gate oxide, generate more oxide charges. From these simulations it arises [50] that the strange GAA behavior is due to a two-dimensional effect similar to the "tip-effect" [51] that enhances the electric field in the corners of the structure.

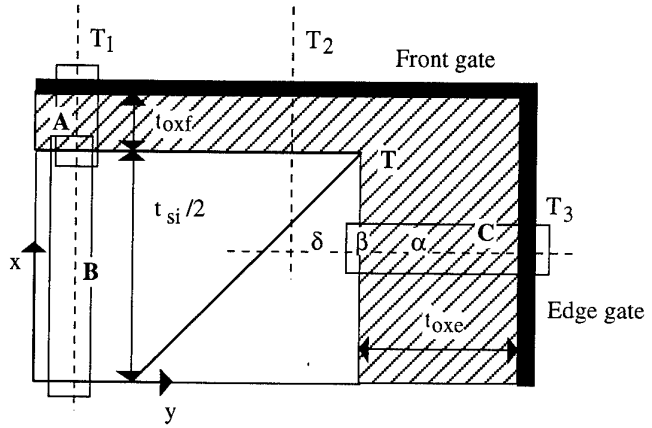

Figure 5.8: Ideal mesa-structure used to compare the edge behavior of GAA and SOI transistors.

The competition between "tip-effect" (dominant in GAA devices) and the increased thickness of the edge oxide (major effect in SOI devices) could be explained by the following general but simple model.

First, considering the main transistor T_1 of Figure 5.8 and applying Gauss' law to the boxes labeled A and B, it comes, at threshold:

$$\begin{aligned} \varepsilon_{si}E_{Sf} - \varepsilon_{ox}E_{oxf} &= Q_{oxf} \\ \varepsilon_{si}E_{Sf} &= Q_{Df} \end{aligned} \qquad (5\text{-}1)$$

with E_{oxf} the electric field across the front oxide, E_{Sf} the front surface electric field, $Q_{Df} = qN_A t_{si}/2$ the depletion charge controlled by the front gate and Q_{oxf} the oxide charges at the front interface. Gauss' law in box C for the edge transistor T_3 gives:

$$\varepsilon_{si}E_{Se} - \varepsilon_{ox}\alpha E_{oxf} = \beta Q_{oxf} \qquad (5\text{-}2)$$

with E_{Se} the edge surface electric field, $\beta Q_{oxf} = Q_{oxe}$ the charges at the edge interface, and $\alpha E_{oxf} = E_{oxe}$ the electric field across the edge oxide. Since the generation of oxide charges is proportional to the oxide thickness, $\beta > t_{oxe}/t_{oxf}$. The inequality is obtained when considering the less quality of the edge oxide which increases the hole trapping factor. Introducing $T > 1$, the "tip-effect" that increases the oxide electric field near the corners of the device, α is given by:

$$\alpha = \left[\frac{V_G - \phi_{ms} - \phi_{se}\left[1+(qD_{it}/C_{ox})\right]}{V_G - \phi_{ms} - \phi_{sf}\left[1+(qD_{it}/C_{ox})\right]}\right]\left[\frac{t_{oxf}}{t_{oxe}}\right] T \approx \left[\frac{t_{oxf}}{t_{oxe}}\right] T \qquad (5\text{-}3)$$

with D_{it}, the density of interface states in $cm^{-2}eV^{-1}$. In (5-3), it has been assumed that the surface potential variation from point to point in the film is a second order effect. T decreases with a $r^{-1/3}$-rule where r is the distance to the corner [51].

When transistor T_1 is at threshold, as it is supposed to be in (5-1), transistor T_3 is already in the "on" state if $\varepsilon_{si}E_{Se} - Q_{De} > 0$ and T_3 is still in the "off" state if $\varepsilon_{si}E_{Se} - Q_{De} < 0$. Q_{De} is the depletion charge controlled by the edge gate. Also, if $\varepsilon_{si}E_{Se} - Q_{De}$ increases(decreases) with dose, the threshold voltage of T_3 is reached earlier(later) relatively to the threshold of T_1.

The combination of (5-1) and (5-2) yields:

$$\varepsilon_{si}E_{Se} - Q_{De} = (\alpha - \delta)Q_{Df} + (\beta - \alpha)Q_{oxf} \qquad (5\text{-}4)$$

with $\delta Q_{Df} = Q_{De}$. Due to the charge sharing between T_2 and T_3, it is generally assumed that the edge transistor controls less charges than the main gate (in a uniformly doped film at least) so that $\delta < 1$. Although δ varies with the distance to the corner, an integral expression of δ could be found in non-fully depleted devices [49] but, to our knowledge, such a calculation has not yet been performed in fully depleted films. In this case, the charge sharing sketched by the oblique line in Figure 5.8 seems generally to provide realistic results. The determination of δ is fortunately not critical in our discussion since it only fixes the relative position of the initial edge threshold voltage compared to the main threshold conduction.

It is clear from (5-4) that the evolution of the edge threshold conduction as a function of dose, which changes Q_{oxf}, is only fixed by $(\beta-\alpha)$:

- In SOI devices, $\beta-\alpha \approx (t_{oxe}/t_{oxf}) - (Tt_{oxf}/t_{oxe})$. $(\beta-\alpha)$ is hence <u>positive</u> as soon as $T < (t_{oxe}/t_{oxf})^2$ which is fulfilled from a short distance of the very corner since t_{oxe} is generally one order of magnitude higher than t_{oxf} (in Figure 5.7: t_{oxf} = 50nm and t_{oxe} = 200nm). Since $\varepsilon_{si}E_{Se} - Q_{De}$ becomes more and more positive when Q_{oxf} is increased, the integral of the edge conduction occurs earlier with dose. The "tip-effect" is masked by the large thickness of the edge oxide. This is exactly what happens with the LOCOS isolation as well.
- On the other hand, in GAA devices, $t_{oxf} = t_{oxe}$ which implies $\beta-\alpha \approx 1-T$. $(\beta-\alpha)$ is <u>negative</u> because T is always superior to unity. $\varepsilon_{si}E_{Se} - Q_{De}$ drops with increasing Q_{oxf} and the edge conduction is delayed upon irradiation: the "tip-effect" becomes dominant.

This model simply demonstrates that, in GAA, the gate control on the edge body potential increases with dose so that no parasitic leakage could appear. The slight increase upon irradiation of the "off" background current (up to 1nA) for negative gate biases observed in Figure 5.5 cannot therefore be attributed to a loss of gate control. It is most likely due to the increase of the fast surface-state density at the Si/SiO_2 interfaces that decreases τ_g, the effective generation lifetime in the space-charged region near the drain. This, in turn, increases the drain junction leakage (as shown by relationship (3-1)).

Finally, (5-3) and (5-4) show that, at first approximation, the delayed build-up of interface states should not change the behavior of the edge conduction.

3.2.3. Electrical parameters up to 85Mrad(Si) irradiation

3.2.3.1. Experimental procedure

^{60}Co gamma irradiations of individual transistors with the gate oxide thickness shrunk down to 30nm will be presented. Devices were kept at room temperature during irradiation which was stopped after 0.066, 0.260, 0.505, 0.790, 1.6, 3.7, 8.7, 17.5, 26.7, 55.6 and 83.4Mrad(Si) to allow measurements. The uncertainty on dose is approximately 20%. The dose rate $\dot{D}$ was progressively increased in order to reduce the time-budget: starting from 3.3rad(Si)/s, $\dot{D}$ has been raised to 6.7rad(Si)/s between 1.6Mrad(Si) and 3.7Mrad(Si) and finally, the rest of the irradiation has been completed with $\dot{D}$ = 11.4rad(Si)/s. The differences between the successive dose rates is too small to significantly influence the results. The duration of the irradiation interruptions dedicated to measurements was kept below two and a half hours. We have verified that no recovery took place within this short period of time. Both 3µm × 3µm n- and p-channel transistors were irradiated with source and drain grounded and with the gate voltage at 0V, 1.5V or 3V. During measurements, the bias has been maintained on all devices except on the one being measured. I_D-V_G curves were recorded by an HP4145 parameter analyzer in linear (V_{DS} = 0.1V) and saturation (V_{DS} = 2V) operation with gate voltage increments of 0.015V (from high to low voltage in absolute value). Linear measurements on n- and p-channel devices biased with the gate voltage at 3V during irradiation are presented in Figures 5.9 and 5.10 respectively. Similar curves are produced in saturation regime. In n-channels, the edge boron implantation helps to delay the parasitic lateral conduction so that the hump visible in Figure 5.5, no longer exists in the logarithmic plot of Figure 5.9 ($V_{th,edge} > V_{th,main} \cong 0.15V$). Obviously, the n-channel threshold voltage rebounds. It is remarkable to note that the edge leakage (and the hump) does not appear after the rebound, which confirms the modest influence of D_{it} on the gate edge control.

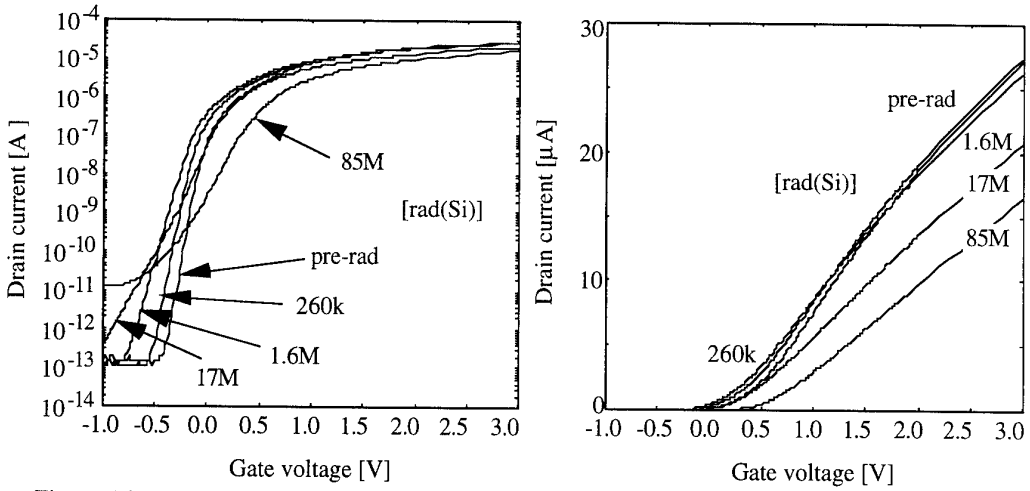

Figure 5.9: Drain current *vs.* gate voltage curves of a 3µm × 3µm nMOS/GAA device exposed to different irradiation doses. $V_S = V_D = 0V$ and $V_G = 3V$ during irradiation, $V_{DS} = 0.1V$ during parameter extraction.

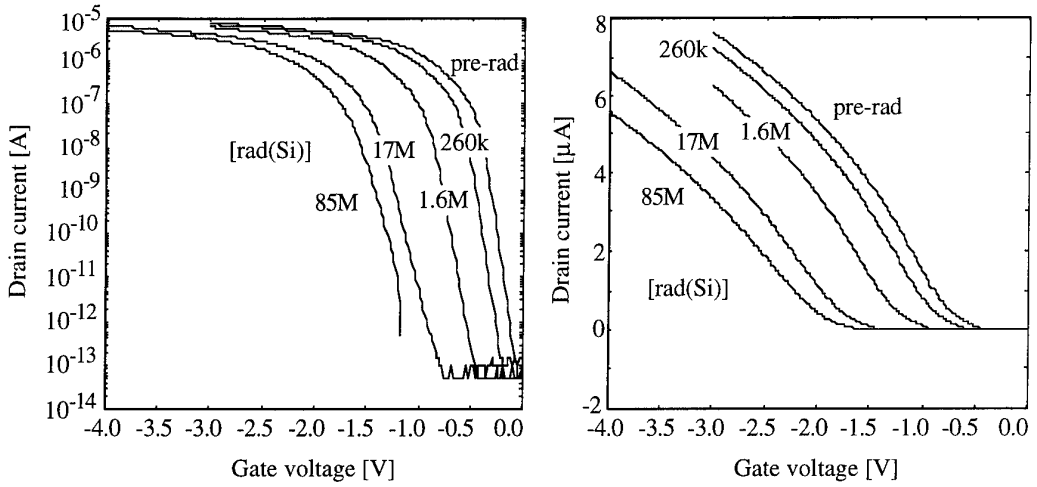

Figure 5.10: Drain current *vs.* gate voltage curves of a 3µm × 3µm pMOS/GAA device exposed to different irradiation doses. $V_S = V_D = 0V$ and $V_G = 3V$ during irradiation, $V_{DS} = -0.1V$ during parameter extraction.

I_D-V_D characteristics were also recorded using V_D and V_G steps of 0.1V and 0.25V, respectively. Some of the results are shown in Figure 5.11 and indicate that both mobility and output conductance decrease under irradiation. The rebound of n-type threshold voltage can also be observed.

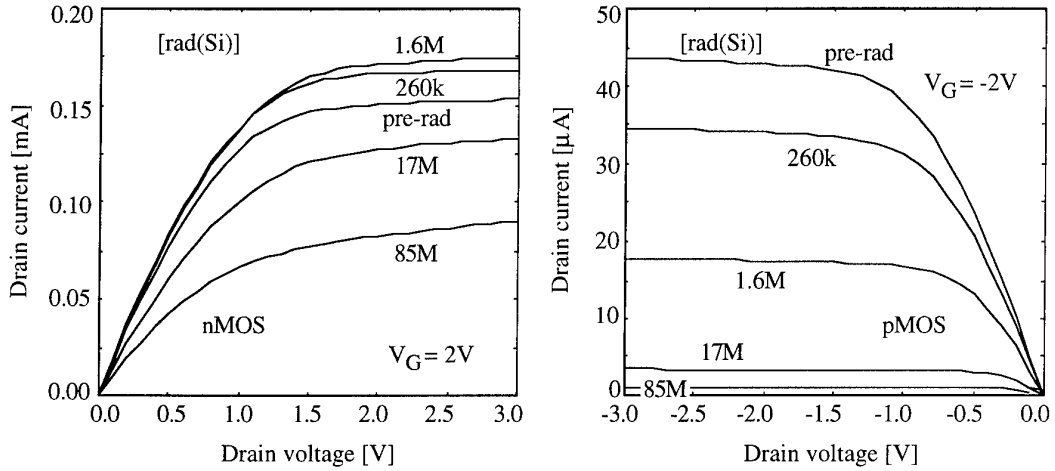

Figure 5.11: Drain current *vs.* drain voltage curves of 3µm × 3µm n- and pMOS/GAA devices exposed to different irradiation doses. $V_S = V_D = 0V$ and $V_G = 3V$ during irradiation, $V_G = \pm 2V$ during parameter extraction.

After 26.6Mrad(Si), the irradiation has been stopped on half of the devices to investigate the effect of an annealing at room temperature. The same bias than during irradiation is applied continuously. Electrical parameters such as the threshold voltage, the transconductance and the output conductance will now be discussed in detail. The results for p-channel accumulation-mode devices are particularly interesting because very few experimental data have been published hitherto.

3.2.3.2. Threshold voltage

Since the edge conduction is delayed, there is no longer a need to extract multiple threshold voltages and very robust methods will be preferred to the maximum transconductance change technique used up to now. The threshold voltage is here defined as the intercept of the V_G-axis by the tangent at the I_D-V_G curve in its inflexion point. Linear operation measurements are considered. This definition gives data in close agreement with the threshold voltage obtained by extrapolation to $I_D = 0$ of the linear least-square fit to the $\sqrt{I_D}$-V_G plot in saturation regime. Figure 5.12 presents V_{thn} and V_{thp} as a function of dose when the gate is maintained at 0V and 3V during irradiation with all other terminals grounded (static bias). Figure 5.12 also presents results with devices mounted in an inverter configuration during irradiation (and dissociated during measurements) and the common gate continuously switched between 0V and 3V at the low frequency of 200Hz. Although, these "dynamic" data were obtained with transistors from another batch and extracted from *in situ* measurements, the comparison with the other "static" data of the same Figure remains valid.

First of all, a comparison between Figure 5.12 and Figure 5.5 allows one to see the huge improvement provided by the reduction of the gate oxide thickness from 50nm to 30nm: with t_{ox} = 50nm, ΔV_{thn} = -1.6V after only 0.6Mrad(Si) (with V_G = 3V during irradiation) while in Figure 5.12, the maximum amplitude of ΔV_{thn} is only ±0.3V up 85Mrad(Si) irradiation. P-channel devices with V_G = 3V and V_{DS} = 0V during irradiation suffer from a more important threshold voltage shift that reaches -1.2V at the highest dose. But they are rarely biased in this way when embedded in digital as well as analog circuits. Figure 5.12 shows that with $V_{GS} = V_{GD}$ = 0V, ΔV_{thp} is much less dramatic and only reaches -0.6V at 85Mrad(Si) irradiation. Furthermore, threshold voltage shifts are also reduced with the gate continuously switched in the inverter configuration.

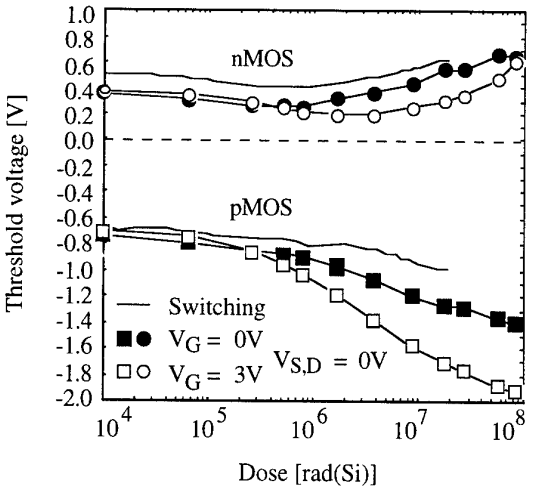

Figure 5.12: Threshold voltage as a function of dose in 3µm × 3µm n- and p-channel GAA devices irradiated with V_G = 0V or 3V and source/drain grounded, or placed in the inverter configuration with the gate continuously switched between 0V and 3V.

We have also observed in both n- and p-type devices, that the threshold voltage shift increases with larger gate electric field, but that the evolution is not linear: there is a

significant difference between V_G = 0V and 1.5V during irradiation but measurements with V_G = 3V only slightly differ from results obtained with V_G = 1.5V, the difference being especially tenuous at low dose. The rebound of V_{thn} is delayed when the gate electric field increases and occurs respectively around 200k, 1.5M and 3.5Mrad(Si) for V_G = 0V, 1.5V and 3V. V_{thp} decreases less rapidly above 10Mrad(Si) irradiation, but neither V_{thn} nor V_{thp} saturates at high doses. After annealing at room temperature during 59 days, V_{thn} and V_{thp} increase by about 0.1V with V_G = 3V (+0.08V in n-channels and +0.14V in p-channels) while threshold voltages are more stable when the gate is grounded (+ 0.02V in n-channels and +0.06V in p-channels). These observations will be easily explained when separating the contribution to the threshold voltage shifts, of interface states and oxide charges.

3.2.3.3. Interface state and oxide-trapped charge effects

Three methods are extensively used in the literature to separate the contributions to the threshold voltage shifts of the charges trapped in the oxide ($\Delta V_{ot} = -\Delta Q_{ox}/C_{ox}$) and of the interface states (ΔV_{it}) with $\Delta V_{th} = \Delta V_{ot} + \Delta V_{it}$. The charge-pumping method [52], although very sensitive, is excluded due to the fact that no body contact can be implemented on GAA structures (separate measurements on gated diodes have not been performed). The subthreshold current stretch-out technique [53] (also called midgap method) could be not reliable enough because of its strong sensitivity to the precise determination of the subthreshold slope. The dual-transistor charge separation technique [54], on the other hand, overcomes the problem related to low-current measurements associated with the midgap technique by assuming that ΔV_{ot} is identical in n- and p-type transistors. When a sufficiently large gate bias is applied during irradiation, this hypothesis is generally assumed to be valid as soon as the processed oxide are the same for both devices. But at small applied electric field, the work function difference between n- and p-channels must be accounted for properly. Fortunately, when using n-type inversion-mode and p-type accumulation-mode transistors, the work function difference between the N^+ polysilicon gate and the P^- active silicon film is nearly identical in both devices since the film boron doping concentration is about the same. This exceptional situation implies that identical gate biases induce identical electric field E_{ox} across the gate oxide in n- and p-channel devices, even if E_{ox} is very small (gate grounded).

The dual-transistor charge separation technique further assumes that interface traps are predominantly charged negatively(positively) in n-channel(p-channel) devices. This method also underlies on the mobility degradation model proposed by Sun-Plummer [55]:

$$\frac{\mu}{\mu_0} = \frac{1}{1+\alpha(\Delta V_{it})} \tag{5-5}$$

where μ_0 is the pre-radiation mobility and α is taken the same for n- and p-channel transistors. From this relationship alone, ΔV_{it} could not be extracted reliably because α is a fitting parameter that depends on the technology. Therefore, using the previously mentioned hypotheses, the dual-transistor method proposes a set of four equations in which α is no longer an adjustable parameter but becomes a variable of the analysis:

$$\Delta V_{itn} = \frac{\beta_n\left(\Delta V_{thn} - \Delta V_{thp}\right)}{\beta_n + \beta_p} \qquad \Delta V_{ot} = \frac{\beta_p \Delta V_{thn} + \beta_n \Delta V_{thp}}{\beta_n + \beta_p}$$

$$\Delta V_{itp} = \frac{-\beta_p\left(\Delta V_{thn} - \Delta V_{thp}\right)}{\beta_n + \beta_p} \qquad \alpha = \frac{\beta_n + \beta_p}{\left(\Delta V_{thn} - \Delta V_{thp}\right)}$$

with

$$\beta_n = \frac{\mu_{n0}}{\mu_n} - 1 \qquad \beta_p = \frac{\mu_{p0}}{\mu_p} - 1$$

For the method to be self-consistent, the value of α must remain approximately constant for all doses which provides an easy check of the results.

The dual-transistor separation of ΔV_{it} and ΔV_{ot}, performed on saturation measurements for both n- and p-channel transistors irradiated with V_G = 3V, is plotted in Figure 5.13 (left). The checking parameter α is shown in Figure 5.13 as well (right) and becomes stable as soon as the dose exceeds 0.1Mrad(Si). The midgap technique has been used independently to confirm that ΔV_{otn} is nearly identical to ΔV_{otp} which gives further confidence in the dual-transistor method.

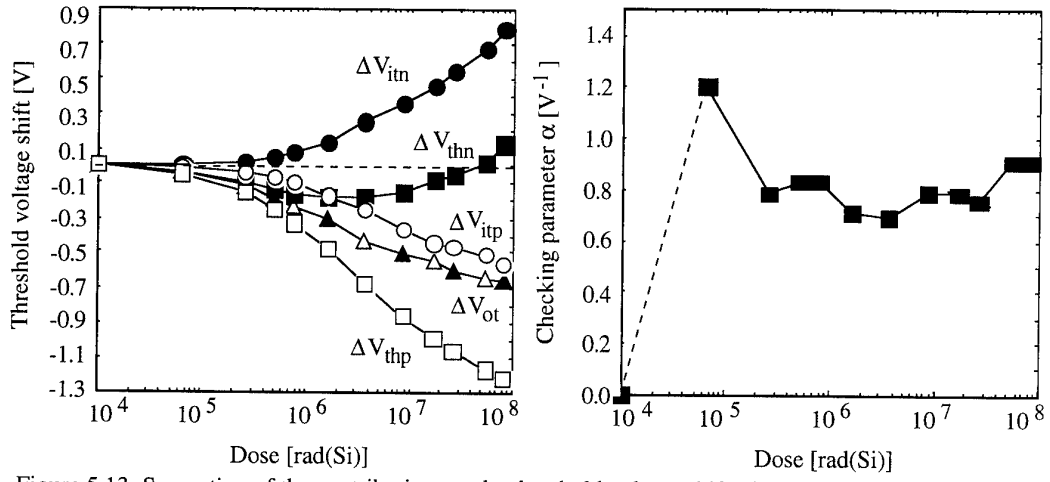

Figure 5.13: Separation of the contributions to the threshold voltage shift of interface states and oxide charges in 3µm × 3µm n- and p-channel GAA devices irradiated with V_G = 3V (left) and checking parameter α (right) as a function of dose.

In both devices, the interface trap generation is delayed (because it has a longer time constant than trapping of positive charges) and increases critically after approximately 1Mrad(Si) irradiation giving rise to the rebound of V_{thn} and to the larger drop of V_{thp}. ΔV_{itn} and ΔV_{itp} are not perfectly symmetrical: $\Delta V_{itn} > |\Delta V_{itp}|$ at each dose. The reason is the following: inversion-mode n-channel and accumulation-mode p-type devices are sensitive near threshold to the number of interface traps in the upper and lower half parts of the silicon bandgap respectively, and it is often observed that the density of interface traps in the upper region of the bandgap is larger than in the lower region [56].

The dependence on gate bias applied during irradiation can be found in Figure 5.14. Both the number of charges trapped in the oxide (squares) and the interface state generation (circles) increase with the gate voltage applied during irradiation. It is also clear that results with V_G = 1.5V and 3V are nearly the same below 10Mrad(Si). This explains why the threshold voltage shifts increase with the gate bias especially at high dose. Depending on the extraction method, the variation of ΔV_{it} with V_G appears at a

lower dose in nMOS devices (when the midgap method is used) or in pMOS devices (with the dual-transistor method). These results are not surprising since no general consensus exists in the literature concerning the sensitivity of the interface trap generation to the gate bias.

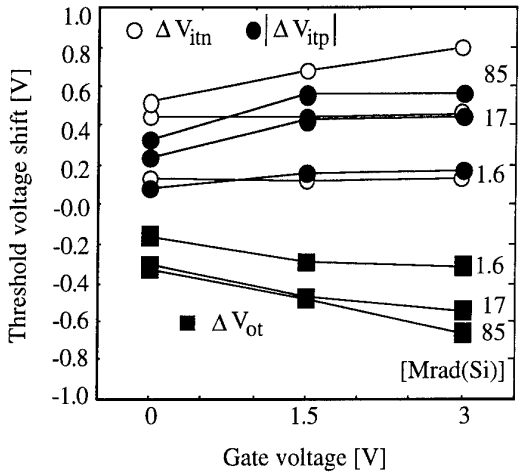

Figure 5.14: Contributions of interface traps and oxide charges to the threshold voltage shifts as a function of gate bias applied during irradiation with dose as parameter in 3μm × 3μm n- and p- channel GAA devices. Dual-transistor extraction method.

Figure 5.14 also shows that the interface state generation does not saturate with increasing dose while charge trapping saturates around 10Mrad(Si) irradiation, the saturation being more pronounced at low gate bias. This is consistent with the observation that V_{thp} continues to decrease steadily up to the highest dose but decreases slowly above 10Mrad(Si).

The dependence of interface state (open dots) and oxide charge (dark dots) contributions to the threshold voltage shifts is presented in Figure 5.15 as a function of the annealing time at room temperature. Interface states do not anneal after the irradiation stop (ΔV_{it} is nearly stable). On the contrary, a very small fraction of them continues to be generated, especially in pMOS devices. This is indicated by the drop of ΔV_{itp} after 384 hours annealing (16 days). On the contrary, a non negligible portion of the trapped charges disappears (ΔV_{ot} increases), this effect being strongly enhanced by a larger electric field. This justifies the 0.1V positive shift of both threshold voltages after the 59-day (1416-hours) annealing with V_G = 3V during irradiation. The rebound of the threshold voltages during annealing is however weakly pronounced because the small dose rate adopted had already favors an on-line annealing during irradiation.

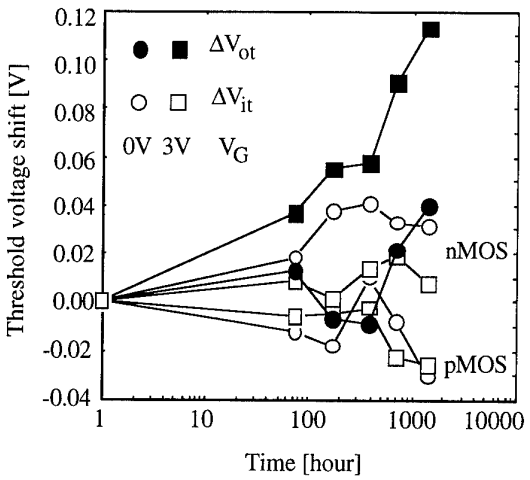

Figure 5.15: Contributions of interface traps and oxide charges to the threshold voltage shifts as a function of annealing time in 3µm × 3µm n- and p- channel GAA devices irradiated with V_G = 0 or 3V. Dual-transistor extraction method.

The density of radiation-induced interface traps ΔD_{it} is obtained from ΔV_{it} by [56] $\Delta D_{it} = C_{ox}\Delta V_{it}/(q\Delta(\psi))$ with $\Delta(\psi)$, in units of eV, the bandgap range over which the interface traps contribute to measurements and C_{ox} the gate oxide capacitance. We assume that the midgap and dual-transistor techniques measure the number of radiation-induced interface traps from midgap to threshold (this assumption is perfectly licit for the midgap technique and provides a good approximation for the dual-transistor method [56]). Midgap corresponds to ϕ_F but the precise location of the surface potential corresponding to the two threshold voltage extractions described above is uncertain. For n-channel transistors, we assume that the surface potential at threshold approximately corresponds to the onset of strong inversion so that $\Delta(\psi) \approx 2\phi_F - \phi_F \approx \phi_F$. For accumulation-mode p-channel transistors, we use $\Delta(\psi) \approx 0 - \phi_F \approx -\phi_F$. Therefore, ΔD_{it} is obtained from ΔV_{it} with the same factor of proportionality in both n- and p-channel devices, only the sign differs. The density of radiation-induced oxide charges ΔN_{ox} is simply given by $-C_{ox}\Delta V_{ot}/q$. ΔN_{ox} and ΔD_{it} obtained after a 26Mrad(Si) irradiation and after a subsequent 1416-hour annealing, are summarized in Table 5.2. ΔD_{it} is characteristic of an unhardened gate oxide which confirms that the geometry of the GAA device alone provides sufficient total-dose hardness although better performance could surely be obtained by further improving the process.

Table 5.2: Densities of interface traps and oxide charges after 26Mrad(Si) irradiation and after a subsequent 1416-hour annealing as a function of the gate bias in 3µm × 3µm n- and p- channel GAA devices.

	ΔD_{it} [cm^{-2} eV^{-1}]				ΔN_{ot} [cm^{-2}]	
	nMOS		pMOS		nMOS = pMOS	
V_G	0V	3V	0V	3V	0V	3V
26Mrad(Si) irradiation	9.0×10^{11}	1.0×10^{12}	4.9×10^{11}	7.7×10^{11}	2.7×10^{9}	4.8×10^{9}
1416h annealing	8.5×10^{11}	9.9×10^{11}	4.4×10^{11}	7.5×10^{11}	2.5×10^{9}	4.0×10^{9}

3.2.3.4. Transconductance and mobility

In linear operation, the mobility μ is defined from (3-2) as the extrapolation to $V_G = V_{th}$ of the best linear fit to the g_m-curve above threshold, divided by $2C_{ox}V_{DS}W/L$. In saturation regime, $\mu = 2m^2L/(C_{ox}2W)$ with m the slope of the linear least-square fit to the $\sqrt{I_D}$-V_G curve. The device width is doubled owing to conduction at the front and back interfaces. Figure 5.16 plots the mobility (left part) and the mobility degradation μ/μ_0 (right part) extracted from saturation measurements as a function of dose with the gate bias as parameter. The mobility degrades upon irradiation due to the creation of interface states as shown in relationship (5-5). The mobility obtained from measurements in linear operation is about 35% larger than from saturation measurements but the degradation with dose is also slightly larger such that less difference between the two definitions is observed at high dose (only 10%).

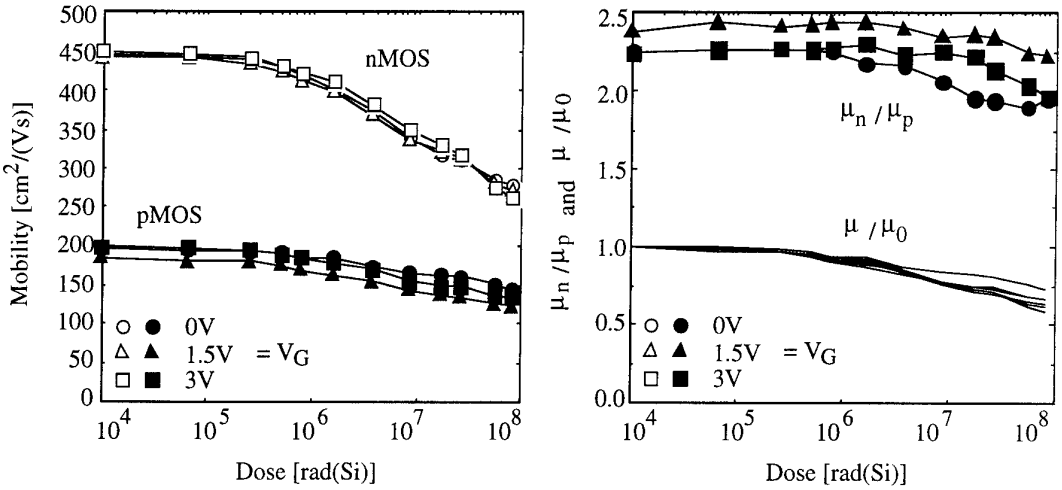

Figure 5.16: Mobility (left) and mobility degradation (right) as a function of dose with gate bias during irradiation as parameter in 3μm × 3μm n- and p- channel GAA devices.
Extraction from saturation measurements.

The influence of the gate electric field applied during irradiation is very weak in nMOS devices as already observed in [57] at lower doses. On the other hand, the mobility degradation is slightly larger with increasing V_G in pMOS transistors (μ_p/μ_{p0} = 81%, 72% and 74% at 26Mrad(Si) with V_G = 0V, 1.5V and 3V, respectively). The mobility remains above 95% of its initial value up to 500krad(Si) and then falls with a slope approximately equal to -17%/decade. Finally, at 85Mrad(Si), the mobility degradation is around 58% and 66% in n- and p-type devices respectively with V_G = 3V during irradiation. The ratio between n and p mobilities remains approximately constant around 2.3 up to 10Mrad(Si) (Figure 5.16, right part) and then slightly falls down to 2. The mobility does not recover with annealing since μ is linked to the interface state generation, stable (or slightly increasing) with time after the irradiation stop.

The mobility reduction factor θ can be extracted from measurements in linear operation. In (3-2), θ is defined as the slope of the best linear fit to the g_m-curve above threshold. As shown in Figure 5.17, θ strongly decreases with dose. The intrinsic mobility reduction coefficient $\theta' = \theta - R_{sd}\mu C_{ox}2W/L$, free of source/drain resistance effects, cannot be extracted because the evolution of R_{sd} with dose is unknown.

However, from simulations, R_{sd} is expected to increase upon the action of interface states and to increase(decrease) in p-channel(n-channel) devices under the influence of oxide charges. The net result should be an increase of R_{sd} at very high doses in both types of devices (when interface states play a dominant part). If this increase of R_{sd} with dose is confirmed, this would mean that the mobility reduction θ' (due to transversal electric field only) decreases faster with dose than θ, and could eventually become negative (mobility enhancement). Clearly, further investigation is required.

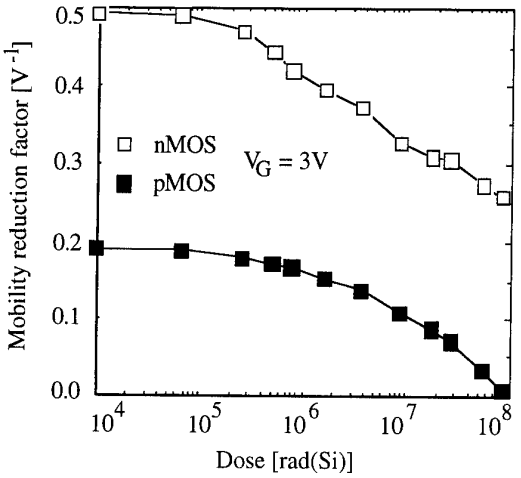

Figure 5.17: Mobility reduction factor as a function of dose in 3µm × 3µm n- and p- channel GAA devices irradiated with V_G = 3V.

3.2.3.5. Subthreshold slope

The subthreshold slope S has been extracted using the 10pA-1nA and 3pA-0.3nA current ranges in nMOS and pMOS, respectively. These ranges have been shifted upwards for very high doses (and become respectively 0.5nA-70nA in nMOS and 10pA-1nA in pMOS) due to the apparition of a breaking point in the subthreshold slope around I_D = 1nA in nMOSFETs and due to the increase of leakage currents up to about 1pA in pMOSFETs (Figures 5.9 and 5.10). These effects are most likely linked to drain junction leakage. Linear and saturation measurements provide the same results.

The subthreshold slope is depicted as a function of total-dose in Figure 5.18. The initial value of S is close to the theoretical limit for both n- and p-channel devices (62mV/dec) owing to the strong control of the surrounding gate on the body potential. It is well-known that S drops under irradiation due to the formation of interface states following relationship (2-28). The degradation after 85Mrad(Si) irradiation is larger in n-type transistors (S = 210mV/dec) than in p-channel devices (S = 110mV/dec) which is not surprising since ΔD_{it} has been shown to be larger in nMOS structures (Table 5.2). Contrarily to what is observed with the mobility, also governed by ΔD_{it}, S clearly depends on the gate bias in n-channel devices. The irradiation produces less degradation with the gate grounded than under high electric field (S = 217mV/dec with V_G = 1.5V and S = 189mV/dec with V_G = 0V after 85Mrad(Si) irradiation). In pMOS devices, on the other hand, the influence of the gate electric field is remarkably negligible. Just like D_{it} and µ, the subthreshold slope does not significantly vary during annealing.

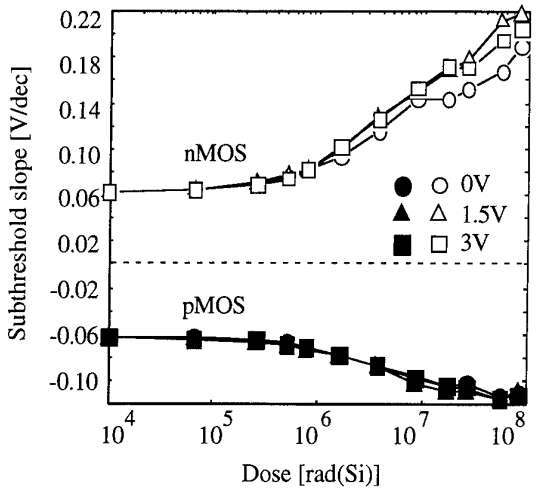

Figure 5.18: Subthreshold slope as a function of dose with gate bias during irradiation as parameter in 3µm x 3µm n- and p- channel GAA devices. Extraction from linear measurements.

3.2.3.6. Implications for analog design

In addition to the threshold voltage and the transconductance, the scaled transconductance g_m/I_D [V^{-1}] and the output conductance $g_D = I_D/V_{EA}$, with V_{EA} the equivalent Early voltage [58], are physical characteristics which are crucial for analog design. Indeed, considering a common-source MOS transistor operating in saturation and loaded by an ideal current source and an output capacitance C_L (Figure 5.19), it is well-known that the transition frequency of the voltage amplification (the frequency where the open-loop gain is equal to unity) is given by $(g_m/I_D)(I_{bias}/2\pi C_L)$, while the D.C. voltage gain A_0 is equal to $(g_m/I_D)V_{EA}$. Variations of the noise characteristics with dose are important as well and can be found in Reference [59] for GAA devices.

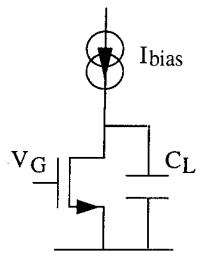

Figure 5.19: MOSFET in basic common-source amplifying configuration.

• Scaled transconductance

The evolution of g_m/I_D as a function of the normalized drain current $I_D/(W/L)$ with dose as parameter is depicted in Figure 5.20 for devices irradiated with V_G = 3V. This parameter is independent on device dimensions and its value inversely follows the inversion level in the silicon film [60]. In weak inversion region, the maximum of the scaled transconductance is related to the subthreshold slope S by $(gm/I_D)_{max}$ = ln(10)/S. Since the pre-radiation value of S is close to the theoretical limit, $(gm/I_D)_{max}$ before irradiation approaches q/kT = 38.4V^{-1}. Like the subthreshold slope, $(gm/I_D)_{max}$ degrades, as shown in Figure 5.21, and falls down to 30% and 50% of its initial value after 85Mrad(Si) irradiation in n- and p-channel devices respectively. The drop is more

rapid in n-channel devices as expected from the larger interface state generation. The scaled transconductance in strong inversion operation ($I_D > 1\mu A$), on the contrary, is nearly not affected by dose up to 85Mrad(Si), and should follow the degradation of the square root of μ. The influence of the gate bias during irradiation is negligible in p-channel devices, and the degradation is slightly smaller with $V_G = 0V$ in n-channel devices.

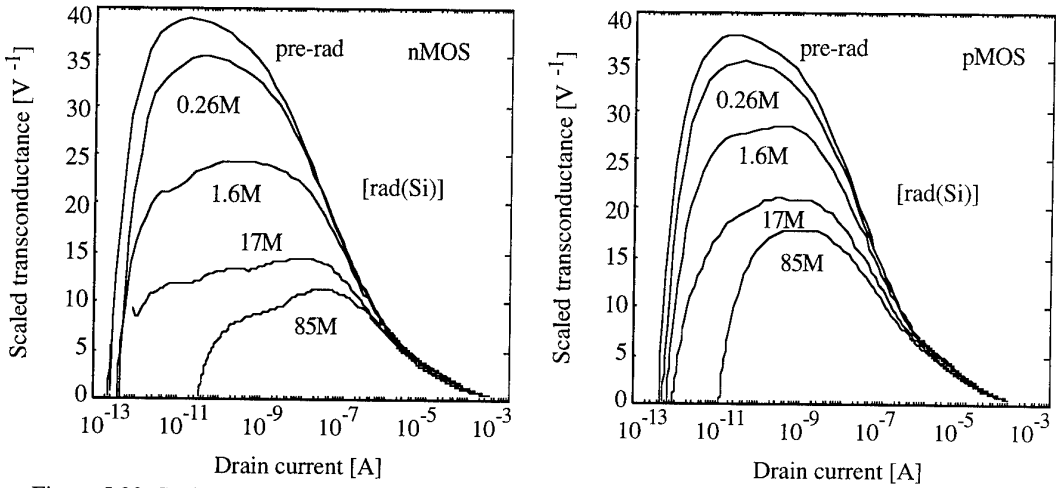

Figure 5.20: Scaled transconductance g_m/I_D as a function of the normalized drain current $I_D/(W/L)$ with dose as parameter in $3\mu m \times 3\mu m$ n- and p- channel GAA devices irradiated with $V_G = 3V$.

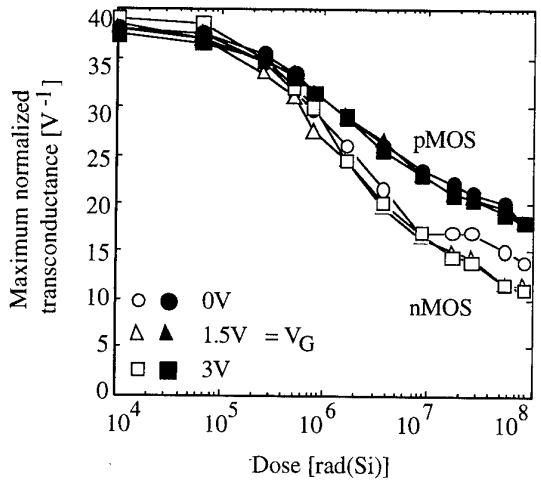

Figure 5.21: Maximum scaled transconductance of $3\mu m \times 3\mu m$ n- and p- channel GAA devices as a function of dose with the gate bias applied during irradiation as parameter.

• Output conductance

The output conductance g_D is obtained as the slope of the best linear regression on the flat portion of drain current *vs.* drain voltage curves presented in Figure 5.11. The lower boundary for V_D ensures that the device is in saturation regime while the upper boundary eliminates the region where impact ionization could appear. Since g_D depends on V_G, three different extraction methods, summarized in Table 5.3, are compared: in the first two cases, V_G is adapted to maintain a constant current level as a function of the dose; in the third case, V_G is kept constant.

Table 5.3: Summary of three different methods to extract the output conductance.

	Method 1	Method 2	Method3
nMOS	$I_D > 40\mu A$	$I_D > 80\mu A$	$V_G = 1.5V$
pMOS	$I_D > 10\mu A$	$I_D > 20\mu A$	$V_G = 1.75V$

The resulting Early voltages $V_{EA} = I_{D0}/g_D$ are shown in Figure 5.22 as a function of dose, with I_{D0} the drain current linearly extrapolated to V_G = 0V. Only small discrepancies appear between the three definitions of V_{EA}, the spread being more pronounced at low(high) doses in nMOS(pMOS) devices (Figure 5.21, left). The pre-rad value of V_{EA} is generally larger in n-channel (60...100V) than in p-channel devices (60...70V). V_{EAn} remains constant up to about 1Mrad(Si) and then severely drops towards a new stable value around 10...20V. The degradation is slightly worst but begins at higher dose with enhanced gate electric field (Figure 5.21, right). The degradation in pMOS devices is much less severe since V_{EAp} is still in the range 35...50V after 55Mrad(Si). Very few results are available in the literature concerning the variation with dose of parameters specific to analog designs, and data about g_D are extremely hard to find. In [57], authors mentioned no significant degradation of g_D up to 10Mrad(Si). Two or three dimensional device simulations should be performed to understand the effect of Q_{ox} and D_{it} on V_{EA}.

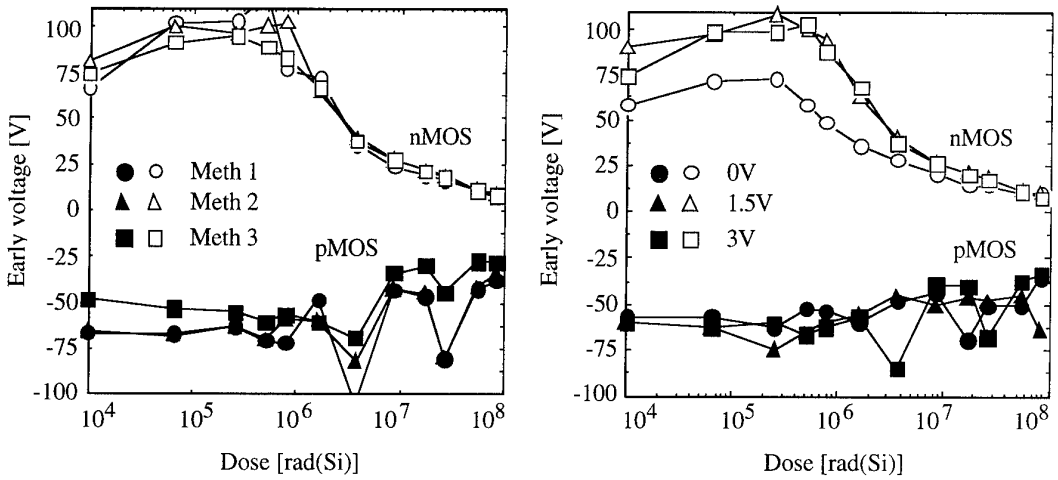

Figure 5.22: Output conductance as a function of dose in 3μm × 3μm n- and p- channel GAA devices with :
Left: three different extraction methods (presented in Table 5.3) as parameter (V_G = 3V during irradiation);
Right: the gate bias during irradiation as parameter (mean value of the three extraction methods).

4. Conclusions

We showed that the GAA structure adds to the many advantages of regular fully-depleted SOI devices, a strong total-dose radiation hardness. In GAA devices indeed, only a thin layer of high quality gate oxide is in contact with the active silicon film. The geometry also ensures that no edge leakage could appear upon irradiation exposure. GAA transistors are therefore promising candidates for digital as well as analog applications at

least up to 100Mrad(Si) irradiation, which meets the requirements of the most advanced nuclear projects. Furthermore, the GAA devices should benefit from a strong SEU hardness because each transistor consists of a very small silicon volume completely isolated from the surrounding devices and the substrate. This will be confirmed in Chapter VII. Chapter VI will deal with circuit skills intended to improve the total-dose hardness of soft processes like the FD SOI technology.

References

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Chapter VI: Total-dose hardness of a 1k GAA SRAM

As far as total-dose is concerned, the future nuclear industry sets the most challenging problems such as the maintenance of fission and fusion reactors. These tasks require the development of teleoperators or robots with a high level of autonomy. Robots gain autonomy owing to various captors which determine position, acceleration, temperature, *etc*. Sometimes, robots should even be provided with a camera allowing remote exploration. Therefore, placing some electronics parts in the "hot" area becomes unavoidable. Indeed, even without considering tele-transmission, some basic analog and digital circuits are required to amplify and multiplex the captor output signals before transmission on long cables. As a consequence, the correct prediction of the performance of complex microelectronic circuits up to very high levels of total-dose irradiation is an essential skill.

This chapter concentrates on the total-dose radiation effects on logic ICs. The main total-dose related failure mechanisms are first briefly reviewed. Next, the efficiency of methods using circuit design skills to improve the total-dose performance of soft processes are discussed. The classical radiation-hard design rules are succinctly recalled. Then, new design considerations for CMOS inverters are presented and shown to be successful to sustain very large negative threshold voltage shifts. Since they consume quite large silicon real estate, these local compensation techniques are nevertheless impractical for the cross-coupled inverters of static memory cells that take most of the SRAM chip area. The stability of the classic six-transistor memory cell is then discussed as a function of dose and a method to determine the optimum size of the different transistors is presented. It is also shown that the optimum cell design unfortunately does not prevent memory failure linked to leakage currents in n-channel devices so that the total-dose radiation hardness mainly relies on the technology. The excellent total-dose behavior up to 85Mrad(Si) irradiation of 1k GAA CMOS SRAMs synthesizes and confirms theoretical expectations.

1. Basic rules

From a circuit design viewpoint, the principal total-dose effects for MOS devices are a negative shift of the threshold voltages (before the possible rebound in n-channel devices) and a reduction of the mobility. For n-channel devices, a negative threshold voltage shift

will increase the drive current (effect which is partially compensated by reduced mobility), and, more importantly, will also increase the off-state leakage current. For p-channel devices, a negative threshold voltage shift will reduce the on-state drive current. Since the threshold voltage shift is enhanced by a positive gate bias, it is generally admitted that n-channel devices, which have a zero or positive gate-to-source bias, have larger threshold shifts than p-channel MOSFETs. Keeping these effects in mind, two types of radiation-induced failure mechanisms can be easily identified [1]: logic-level failures and timing failures.

- Logic-level failures occur if the combination of the increased n-channel leakage current with the decreased p-channel drive prevents the signal at a critical node from reaching a valid "high" logic level. The sensitivity of a node is evaluated by the ratio of the maximum n-path leakage to the minimum p-path conductance. Logic-level failures occur in poorly ratioed logic gates such as NOR gates with small p-channel transistors. Therefore, experimental results demonstrate high noise immunity, high packing density and high speed superiority of NAND gates (where the n-channel transistors are in series and the p-channel transistors are in parallel) to NOR gates (where the opposite arrangement is found) for design hardening [2]. Generally the ratio of pMOS size to nMOS size is determined so that the pre-radiation signal data fall time would be equal to the post-radiation signal data rise time [3]. The worst-case bias conditions are with n-channel transistors "on" and p-channel transistors "off" during the irradiation.

- Timing failures occur when the degradation of the current drive of p-channel transistors (or n-channel devices after the rebound) leads to a degraded (too slow) "low"-to-"high" ("high"-to-"low") transition. The added delay introduced by this degradation can result in failure at a point in the circuit or at some other point farther along the signal path.

The worst-case bias conditions are the same than for logic-level failures. Timing failures depend not only on the n- to p-channel size ratio, but are also influenced by the circuit nodal capacitances. It should be noted that reducing the gate oxide thickness to improve the radiation hardness induces an increase of the nodal capacitances which might actually tightens the tolerance to timing failures. Generally, synchronous circuits are preferred to asynchronous designs because the regular clocked timing can be slowed down to avoid timing failures [4]. Also, because the maximum operating frequency decreases while the minimum refreshing frequency of dynamic circuits should increase (to overcome n-channel leakage), fully static circuits, though carrying an area penalty due to extra transistors required, are more robust against radiation effects that dynamic circuits [3,4].

Additional failure mechanisms are related to the threshold shift variations which can appear between different transistors of the same type in a circuit, as a function of the local bias during irradiation. The two cross-coupled inverters of a static RAM cell for example have opposite biases. If the memory cell stays in a given state for a long time during irradiation, the "imprinting" of this state will occur and the opposite state could ultimately not be written anymore [5]. Also differential circuits (such as differential sense amplifiers)

often have performance dictated by relative transistor thresholds, so that the designer should attempt to keep the circuit under uniform bias conditions as large a percentage of time as possible.

In the following, abundant theoretical considerations for logic-level failure suppression will be discussed, starting from the simplest logic blocks up to the design of a full 1k SRAM. The proposed techniques are useful to harden enough very sensitive technologies (such as fully-depleted SOI circuits). Unfortunately, design modifications intended to stabilize the circuit characteristics upon irradiation exposure, are usually detrimental to compactness and speed. Therefore, the hardening-by-design approach should be only used when no radiation-hard technology is available.

2. Threshold-voltage-variation insensitive CMOS logic

Since threshold voltage shifts are generally the most severe radiation-induced effects in SOI, the design of radiation hard circuits can be simplified to the design of threshold-voltage-variation insensitive circuits. Large negative threshold voltage shifts are of concerned due to the large charge buildup in the buried oxide. Then, if interface state generation becomes dominant, large positive rebound of V_{thn} should be investigated as well. Usually, in SOI circuits, the largest pressure for failure is quiescent current increase before the rebound of V_{thn}. Too much power drawn is usually a big killer.

Several design strategies have been previously proposed. One possible solution is the back-gate bias generator (BGBG) [6]. The operation of the BGBG is based on the observation that charges trapped in the buried oxide can be balanced by the use of a negative back-gate bias. The threshold shift caused by irradiation is then compensated by using a circuit that senses this shift and changes the back-gate voltage accordingly. By integrating this circuit together with the application circuit it is possible to compensate threshold voltage changes for an entire chip. The drawback of the method is that it is restricted to the SOI technology. Furthermore, it considers that all the transistors integrated on the same chip are submitted to the same threshold voltage shift, which is obviously not the case (due to the local variation of the bias during irradiation). Also, the substrate- and gate-to-source voltages are not identical for all transistors embed in a complex circuit so that the ideal correction of the threshold voltages should not be really uniform. Another solution is to develop a compensation circuit that could be added to each inverter, NOR or NAND gate to locally compensate for the threshold voltage shifts and stabilize the output characteristics.

2.1. Theoretical considerations

In order to produce adequate compensation solutions, it is necessary to understand the basic total-dose degradation mechanisms of a CMOS inverter. Before the possible rebound of V_{thn}, n- and p-channel threshold voltages shift both towards more negative values. Figure 6.1 presents Spice-simulated transfer characteristics of an inverter for different values of V_{thn} and V_{thp}. As usually admitted, the V_{thp} shift is taken smaller than the V_{thn} shift and the Figure has been arbitrarily plotted for $\Delta V_{thn} = 4\Delta V_{thp}$.

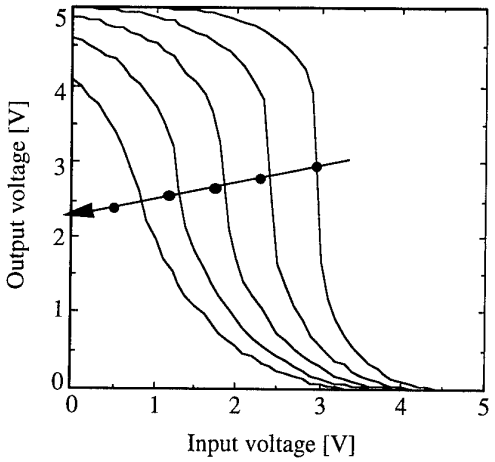

Figure 6.1: Simulated transfer characteristics of a classical CMOS inverter. V_{thn} ranges from 1 to -3V per 1V steps and V_{thp} ranges from -0.5 to -1.5V per 250mV steps, from right to left along the arrow. V_{dd} = 5V. $(W/L)_N$ = 1 and $(W/L)_P$ = 3.

Two irradiation effects are remarkable. Firstly, a shift of the transfer characteristic to the left is observed. Secondly, the output "high" logic level becomes lower than the supply voltage as soon as the n-channel threshold voltage is negative. The noise margin of the input at low-state and at high-state decreases and increases respectively upon irradiation.

The dependence of the inverter switching point on V_{thn} and V_{thp} can be quickly estimated by assuming that, at switching, for an output voltage close to half the supply voltage V_{dd}, both n- and p-channel transistors are saturated. This hypothesis is valid as long as V_{thn} is not too negative. The saturation currents I_{sat} are approximated by:

$$I_{satn} = \beta_n \frac{(V_{in} - V_{thn})^2}{2n}$$

$$I_{satp} = \beta_p \frac{(V_{dd} + V_{thp} - V_{in})^2}{2n}$$

where $\beta = \mu C_{ox}(W/L)$, with V_{in} the input voltage, and n is the body effect factor (n = 1 in GAA transistors and is around 1.05...1.1 in SIMOX devices). For simplicity we consider that β and n are identical in n- and p-channel devices. Then by equating the currents in the transistors, it comes that the inverter switches for an input voltage V_{sw} equal to:

$$V_{sw} = 0.5V_{dd} + 0.5V_{thn} + 0.5V_{thp} \qquad (6\text{-}1)$$

Therefore, $\Delta V_{sw} = 0.5\Delta V_{thn} + 0.5\Delta V_{thp}$ which is in fair agreement with Spice simulations as indicated by the dots along the arrow of Figure 6.1. The aim of the compensation circuit is to make ΔV_{sw} as little correlated as possible to ΔV_{thn} (assuming $\Delta V_{thn} >> \Delta V_{thp}$) and to maintain the "high" output level as close as possible to V_{dd}. This implies a tight control of the n-channel drive capability in both "on" and "off" states.

Such an approach has already been investigated in Reference [7].

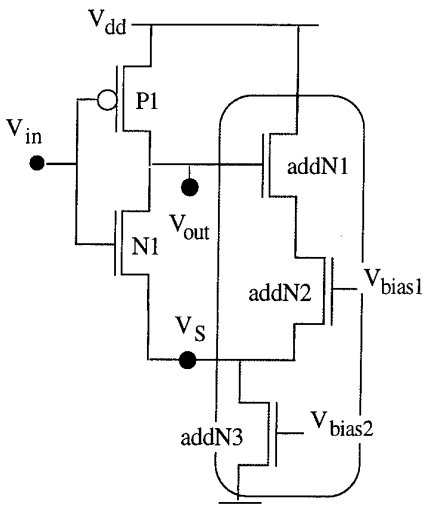

Figure 6.2: Threshold-voltage-variation insensitive CMOS inverter from [7].

The proposed additional compensation circuit, depicted in Figure 6.2, raises the source potential V_S of the main n-channel device N1 accordingly to the drop of V_{thn}. Doing this, the drive capability of N1, proportional to $(V_G-V_S-V_{thn})$, could be maintained quite stable. In particular, leakage currents are avoided when $V_G = 0V$ which leads to a correct "high" output voltage. Nevertheless, the fine compensation presented in Figure 6.2 requires complicated dose-variable bias generation circuits to produce adequate V_{bias1} and V_{bias2}.

2.2. New compensation circuits

Two new simpler designs will be investigated here. The first solution (shown in Figure 6.3, Type-1 inverter) combines a pull-up p-channel transistor (addP) and an n-channel device (addN) inserted below the source of the main transistor N1. The additional circuit controlling V_S is simply commanded by the input voltage. The second solution introduces a pair of complementary transistors in the static diode configuration between the main inverter and the supply lines (Figure 6.3, Type-2 inverter).

• The "pull-up" configuration

When the input voltage is high in the "pull-up" configuration (Type-1 inverter), the additional p-channel transistor addP is "off", addN is "on" and the initial circuit operation is not affected except that transistors addN and N1 are now in series. The new circuit is therefore slower but this drawback may be overcome by doubling the size of each n-channel device. When the input voltage is low, on the other hand, the additional p-channel transistor pulls V_S up to a higher level. As a consequence N1 is more efficiently turned off. The transfer characteristic obtained with this circuit is depicted in Figure 6.4 for the same threshold voltages as in Figure 6.1. Provided that the (W/L) ratio of addP is at least (μ_n/μ_p) times larger than the (W/L) ratio of addN, the improvement is obvious: the "high" output logic level is now very close to V_{dd} even when the threshold voltage of the n-channel devices is strongly negative. As a consequence, the shift of the switching point is also slightly reduced.

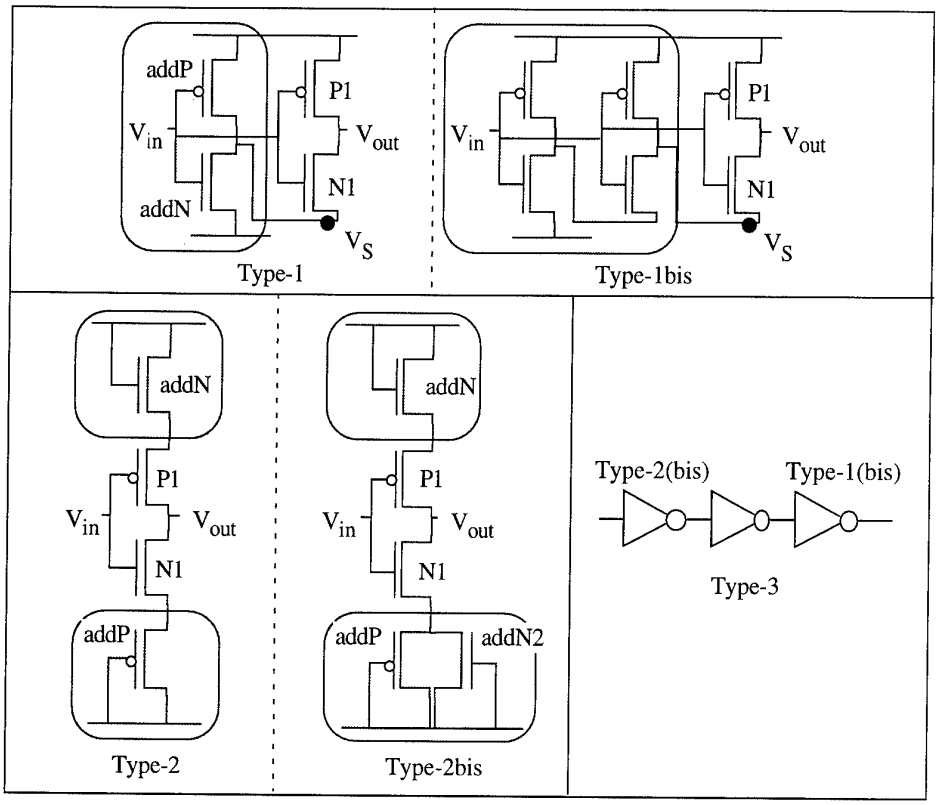

Figure 6.3: New compensation circuits: Types-1 and -1bis are of "pull-up" scheme,
Types-2 and -2bis are of the "diode-pair" scheme.
Type-3 consists of one Type-2bis inverter in cascade with two Type-1bis inverters to form a buffer.

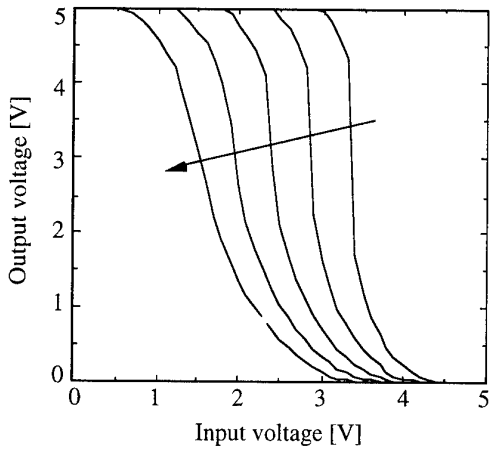

Figure 6.4: Simulated transfer characteristics a Type-1 inverter.
V_{thn} ranges from 1 to -3V per 1V steps and V_{thp} ranges from -0.5 to -1.5V per 250mV steps.
V_{dd} = 5V. $(W/L)_{N1}$ = 1, $(W/L)_{P1}$ = 3, $(W/L)_{addN}$ = 1 and $(W/L)_{addP}$ = 3.

The input switching voltage of the Type-1 inverter can indeed be derived as follows. It is reasonable to assume that, at switching, N1, P1 and addP operate in saturation and addN is in the triode regime. Saturation currents have already been presented. The current in addN can be approximated by:

$$I_{addN} = \beta_{addN}\left[(V_{in} - V_{thn})V_S - \frac{n}{2}V_S^2\right]$$

with V_S, the source voltage of N1. Considering that $\beta_{N1} = \beta_{addN} = \beta_{P1} = \beta_{addP}$, transistor addN drives twice the current flowing in the other transistors and V_{sw} becomes:

$$V_{sw} = \frac{3-\sqrt{3}}{2}\left(V_{dd} + V_{thp}\right) + \frac{\sqrt{3}-1}{2}V_{thn} = 0.634\left(V_{dd} + V_{thp}\right) + 0.366V_{thn} \qquad (6\text{-}2)$$

The body factor is again the same for all transistors. The formula supports and explains the results of Figure 6.4: due to the larger V_{dd} dependence of V_{sw} in (6-2) than in (6-1), the initial transfer curve of the Type-1 inverter is situated to the right of the initial inverter characteristic depicted in Figure 6.1. In addition, ΔV_{sw} is lower for the Type-1 circuit than for the classical inverter in the case of a V_{thn} variation larger than the V_{thp} variation.

The Type-1 inverter can further be improved by using two "pull-up" structures (Figure 6.3, Type-1bis inverter). This design is however quite area-consuming, especially if no reduction of the speed performance is allowed.

• The "diode-pair" configuration

The other simple compensation circuit encloses the initial inverter between a p-channel and an n-channel transistor in the diode configuration (Type-2 inverter). The transfer characteristic of this inverter, presented in Figure 6.5, shows that the "high" output logic level is V_{dd}-V_{thn} as long as $V_{thn} > 0$, and that the "low" output level is not equal to zero but to -V_{thp}. As a function of irradiation dose, the "high" logic level improves as long as V_{thn} drops down to zero and then slightly degrades again when V_{thn} becomes negative. The "low" logic level monotonously increases.

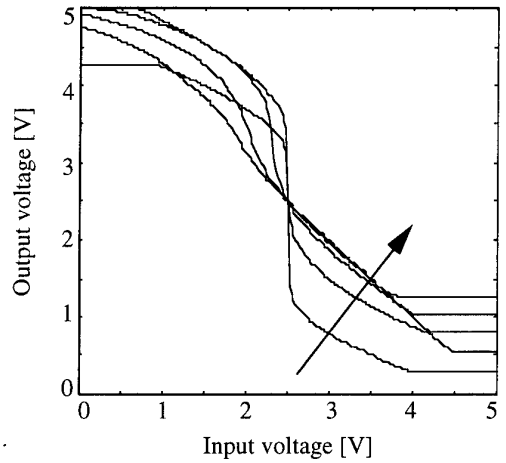

Figure 6.5: Simulated transfer characteristics of a Type-2 GAA inverter.
V_{thn} ranges from 1 to -3V per 1V steps and V_{thp} ranges from -0.5 to -1.5V per 250mV steps. V_{dd} = 5V. $(W/L)_{N1}$ = 1, $(W/L)_{P1}$ = 3, $(W/L)_{addN}$ = 1 and $(W/L)_{addP}$ = 3.

The advantage brought by the circuit is that the shift of the switching point is drastically reduced. Indeed, provided that $(W/L)_{addN} = (W/L)_{N1}$ and $(W/L)_{addP} = (W/L)_{P1}$, the symmetry of the design clearly implies that the transfer characteristic includes the point $V_{in} = V_{out} = V_{dd}/2$ whatever the values of V_{thn} and V_{thp}. In order to improve the "low" logic output, another n-channel device (addN2) can be added in

parallel to addP. The Type-2 inverter then becomes the Type-2bis inverter in Figure 6.3. However addN2 will increase the shift of the switching point when V_{thn} becomes negative.

• Cascade of "diode-pair" and "pull-up" circuits

A nearly perfectly stable transfer characteristic can be obtained as shown in Figure 6.6 by combining the advantages of both the "diode-pair" and the "pull-up" configurations in a three-stage buffer (Figure 6.3, Type-3 buffer).

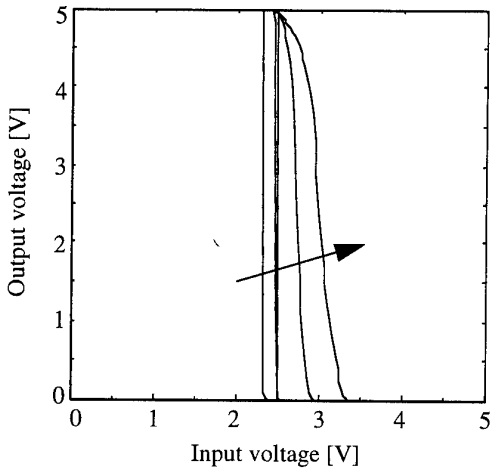

Figure 6.6: Simulated transfer characteristics of a Type-3 buffer constituted by the chain of Type-2, Type-1 and Type-1 inverters. V_{dd} = 5V. V_{thn} ranges from 1 to -3V per 1V steps and V_{thp} ranges from -0.5 to -1.5V per 250mV steps.

A Type-2(bis) inverter is used as first stage to reduce the lateral shift of the transfer characteristic while the last stage is formed by a Type-1(bis) inverter that maintains acceptable "high" and "low" output levels. The middle stage has a weak influence on the results but Type-1 should be preferred to Type-2 at very large threshold voltage shifts.

All the proposed inverter structures consume more silicon real estate than the simple reference inverter, which is the price to pay for increased tolerance to threshold voltage shifts. With the sizes summarized in Table 6.1 (corresponding to the smallest hardening-efficient circuits), Type-1, Type-1bis, Type-2, Type-2bis and Type-3 inverters consume areas which are 1.4, 2.6, 2.2, 3.5 and 9.2 times larger than that of the reference inverter, respectively. The previous estimation has been performed with the very conservative GAA design rules described in Chapter I, and is therefore probably quite pessimistic. Speed is also degraded when using the hardened designs: considering the charge of an output capacitance equal to 0.1pF and with V_{thn} = 0.5V, V_{thp} = -0.5V and V_{dd} = 5V, falling times are equal to 2ns, 3.5ns, 6ns, 24ns, 24ns and 4.5ns respectively from top to bottom in Table 6.1. The simple "pull-up" configuration (Type-1) is therefore about 2 times slower than the reference inverter due to the two n-channel devices placed in series. On the other hand, the "diode-pair" configuration is obviously very bad as far as speed is concerned, being 10 times slower than the reference circuit. Finally, the Type-3 buffer of Figure 6.6 introduces a 35ns-delay in the output response.

Table 6.1: Transistor sizes, total area and falling time on a 0.1pF loading capacitance of the different types of inverter. V_{dd} = 5V.

(W/L)	N1	P1	addN	addP	addN2	addP2	Area	τ fall
Normal	1	2					1	2ns
Type-1	1	1	1	2			1.4	3.5ns
Type-1bis	1	1	1	2	1	2	2.6	6ns
Type-2	1	2	1	2			2.2	24ns
Type-2bis	1	2	1	2	1/3		3.5	24ns
Type-3	Type 2bis --- Type 1bis --- Type 1bis						9.2	4.5ns

The "diode-pair" technique can be easily extended to any other logic block replacing the inverter N1-P1. On the contrary, since the bias of the "pull-up" compensation circuit is controlled by the input voltage, *n* "pull-up" pairs should be added to a *n*-input NAND or NOR gate which is impossible to realize in practice as soon as *n* exceeds 2. However, the "pull-up" configuration can be usefully applied to other circuits such as differential sense amplifiers for example, as shown in Figure 6.7.

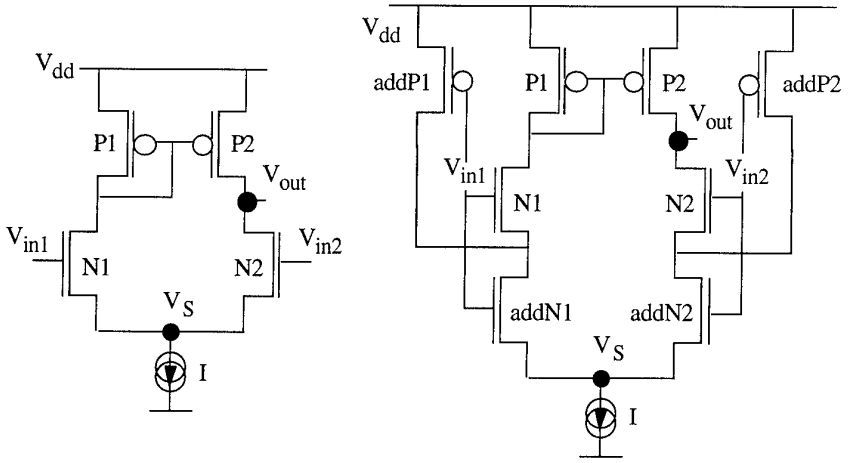

Figure 6.7: Differential sense amplifier: normal version on the left and modified version by addition of the "pull-up" configuration on the right.

The output voltage of the differential sense amplifier is presented in Figure 6.8 as a function of one input voltage, the other input being maintained at V_{dd}. With $V_{in1} = V_{in2} =$ 5V, $(W/L)_{P1,P2}$ is adjusted so that V_{out} is close to $V_{dd}/2$. This point drops when threshold voltages shift because the n-channel drive capability grows while the p-type currents decrease. Keeping V_{in2} at 5V, V_{out} tends to zero when V_{in1} is swept down to 0V. When thresholds shift, the "low" output voltage increases because the leakage current of N1 also flows through the non-zero output impedance R_{dI} of the current source (Figure 6.7). The "high" output voltage, obtained with V_{in1} = 5V and V_{in2} = 0V also degrades when the leakage current of N2 flows through P2 and R_{dI}. It is clear in Figure 6.8 that the "pull-up" configuration allows to conserve correct discrimination between "high" and

"low" output levels even for the largest threshold voltage shift as soon as the lower input voltage is below 1V.

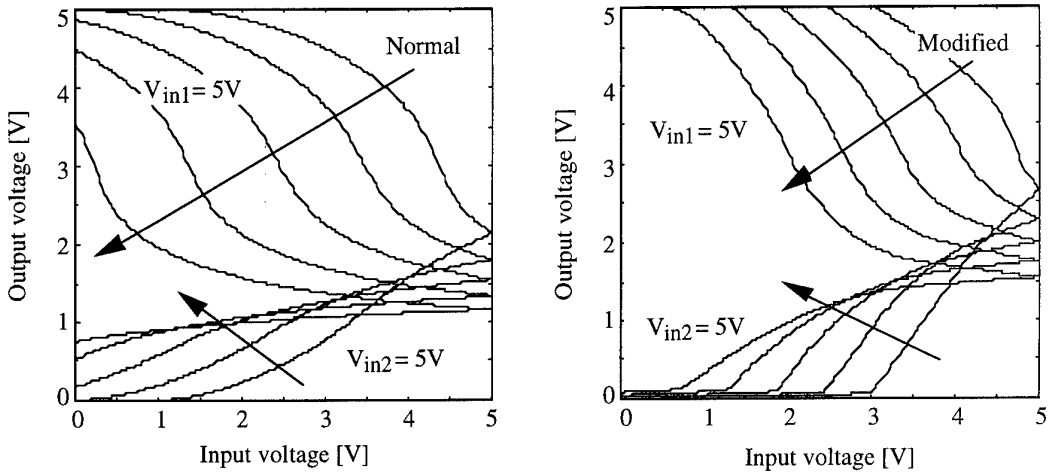

Figure 6.8: Simulated transfer characteristic of a differential sense amplifier. Left: normal version. Right: modified version. V_{dd} = 5V. V_{thn} ranges from 1 to -3V per 1V steps and V_{thp} ranges from -0.5 to -1.5V per 250mV steps. $(W/L)_N$ = 1, $(W/L)_P$ = 3, $(W/L)_{addN}$ = 1 and $(W/L)_{addP}$ = 3.

2.3. Experimental validation

The different types of inverters presented in Figure 6.3 with the size mentioned in Table 6.1 were tested for their sensitivity to threshold voltage shifts. Such shifts can, of course, be obtained by irradiation, but also by varying the back-gate bias of SOI circuits. Indeed, the threshold voltage of both n- and p-channel fully depleted SOI transistors shifts to more negative values when a positive back-gate bias is applied. Thus, the radiation behavior of the compensation circuits can be estimated with no need to perform an actual irradiation.

2.3.1. Back gate bias shift in SOI

Figure 6.9 presents the transfer characteristics of the different types of SOI inverters for a supply voltage of 3V and for back-gate biases V_{BG} of 0V and 20V. Since the buried oxide thickness is 390nm, a back-gate bias shift of 20V corresponds to a positive charge build-up $N_{ox} = 1.1\times10^{12}$ cm^{-2} at the Si/SiO_2 back interface (with $\Delta V_{th} \cong qN_{ox}/C_{ox}$). Note that the shapes of the output characteristics are slightly different in Figure 6.9 and in Figures 6.1, 6.4, 6.5 and 6.6 because neither the supply voltage nor the device parameters, such as transconductances, initial threshold voltages and threshold voltage shifts, do correspond. It is obvious that, after back-gate voltage shift, all types of modified inverters present better characteristics than the normal inverter. For instance, the output voltage of the reference inverter corresponding to V_{in} = 0V drops down to 0.7V when V_{BG} = 20V so that this inverter is clearly no longer functional. All the other types of inverters, on the other hand, are still efficient with the best noise margin of the input at low-state obtained with the Type-3 inverter.

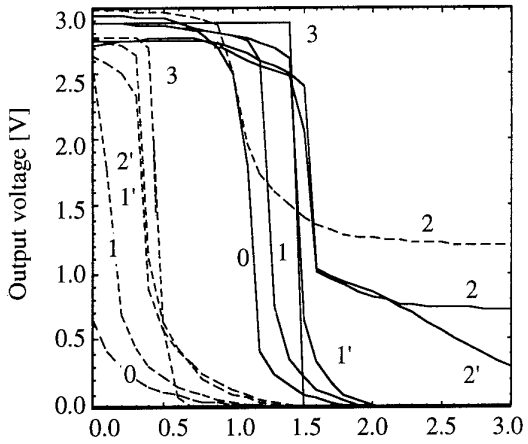

Figure 6.9: Transfer characteristics of the different types of SOI inverters for back-gate biases of 0V (plain lines) and 20V (dashed lines). V_{dd} = 3V. 0: Classical, 1: Type-1, 1': Type-1bis, 2: Type-2, 2': Type-2bis, 3: Type-3 inverters.

The "high" output logic level is plotted in Figure 6.10 as a function of the back-gate bias. The threshold voltages of the SOI n- and p-channel devices vary almost linearly from 0.55V to -1V and from -1.1V to -1.85V, respectively, as the back-gate voltage is swept from 0V to 20V. At high back-gate bias (V_{BG} > 12V), all the proposed inverter structures behave in a better way than the reference inverter. As expected, it can be seen that the "high" output level of Type-2 and Type-2bis inverters first improve when V_{thn} is reduced down to zero. The Type-2 inverter shows the best stability of the "high" output level because there is no direct n-leakage path between V_{dd} and ground, but unfortunately, it presents a degraded "low" output level for all back-gate bias conditions (Figures 6.9 and 6.10). As intended, the design modification of the Type-2bis inverter improves the "low" logic level which is 0.28V when V_{BG} = 0V, and drops to 0V as soon as V_{BG} > 1V. The price to pay is a larger degradation of the "high" logic output.

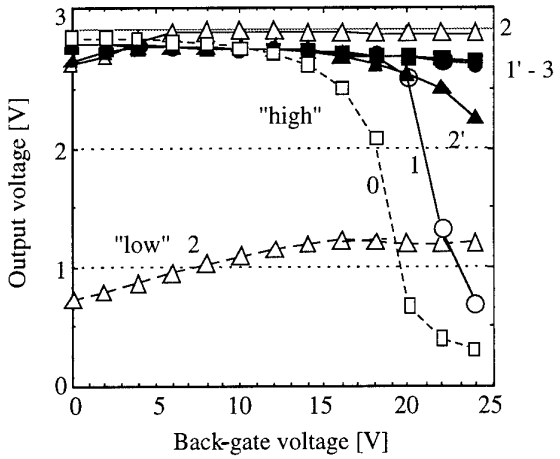

Figure 6.10: "High" output voltage of all SOI inverters (for V_{in} = 0V) and "low" output level of the Type-2 SOI inverter (for V_{in} = 3V) as a function of the back-gate voltage. V_{dd} = 3V. 0: Classical, 1: Type-1, 1': Type-1bis, 2: Type-2, 2': Type-2bis, 3: Type-3 inverters.

Type-1, Type-1bis and Type-3 inverters, on the other hand, always reach a "low" output voltage of 0V as does the reference inverter. Type-1bis (which is also the last stage

of Type-3) furthermore presents a quite good stability of the "high" output which stays above 2.8V when V_{BG} = 20V. This inverter therefore best preserve both "low" and "high" output states and offers the largest output dynamic.

Another important parameter is the shift of the transfer characteristics to the right presented in Figure 6.11 for all structures. This shift is measured as the shift of the input voltage that corresponds to an output voltage of $V_{dd}/2$. It can be seen that the degradation is the worst in the case of the reference inverter (dotted line). Type-1 and Type-1bis present a similar degradation. The improvement when compared to the reference inverter is not as impressive as previously predicted by the Spice simulations. This may be related, using formula (6-2), to the larger variation of V_{thp} compared to V_{thn} with the back-gate bias than the variation considered in simulations ($\Delta V_{thn} = 2\Delta V_{thp}$ experimentally and $\Delta V_{thn} = 4\Delta V_{thp}$ in simulations). The "diode-pair" configuration of the Type-2 and Type-2bis inverters significantly stabilizes the shift of the switching characteristic. This improvement is also found in the Type-3 buffer which contains Type-2bis inverters as first stages. However, the transfer characteristic of the Type-2bis inverter shifts, as predicted, more rapidly once V_{thn} becomes negative, which occurs for a back-gate bias larger than 8V.

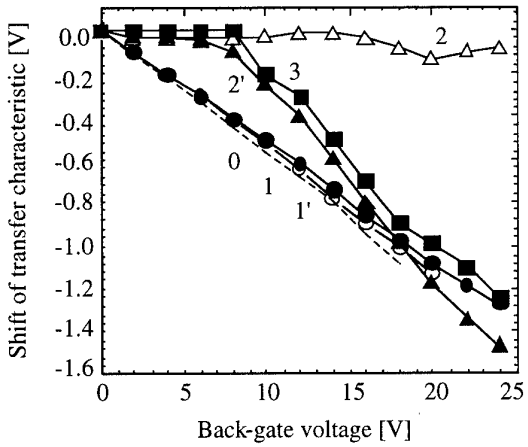

Figure 6.11: Shift of the transfer characteristics (measured at $V_{out} = V_{dd}/2$) as a function of back-gate bias, for the different types of SOI inverters. V_{dd} = 3V. 0: Classical, 1: Type-1, 1': Type-1bis, 2: Type-2, 2': Type-2bis, 3: Type-3 inverters.

In conclusion, Figures 6.9, 6.10 and 6.11 clearly confirm that the "pull-up" configuration (Types-1 and 1bis) improves the logic swing, while the "diode-pair" (Types-2 and 2bis) reduces the shift of the transfer characteristic. Being a combination of "pull-up" and "diode-pair" circuits, the Type-3 buffer presents both improvements at least up to V_{BG} = 15V.

2.3.2. Irradiation of GAA circuits

The different inverter structures (Figure 6.3 and Table 6.1) were also realized with the GAA process and irradiated using a ^{60}Co-γ source with a dose rate of 4rad(Si)/s. *In-situ* measurements were performed up to 2.3Mrad(Si) at time intervals corresponding to desired total-dose values. The pre-radiation threshold voltage of the n- and p-channel

devices were 0.4 and -0.7 V, respectively. The n-channel devices, irradiated under a gate bias of 3V with all other terminals grounded, presented threshold voltages of 0.25, 0.25 and 0.32V for doses of 0.3, 1 and 2.3Mrad(Si), respectively. For the same doses, the threshold voltage of the p-channel transistors irradiated with all terminals grounded was -0.82, -0.9 and -0.93V, respectively. Since the shift of the threshold voltages were relatively modest compared to those obtained by varying the back-gate bias in fully depleted SOI devices, all inverters kept their initial logic levels during the irradiation. A small shift of the transfer characteristics has nevertheless been observed, this shift being again defined for an output voltage of $V_{dd}/2$. The supply voltage was 3V during the irradiation and the input voltage of the inverters was held at either 0V or 3V. Figure 6.12 presents the shift of the characteristics as a function of the irradiation dose for inverters with a 0V-input voltage on the left, and 3V-input voltage on the right. In the worst-case 3V-input bias, the classical inverter only undergoes a 0.25V left shift of its transfer characteristic which should be tolerable in most circuit designs. However, if a more stable transfer curve is to be obtained, some compensation circuits are still useful. As observed previously, the "diode-pair" configuration (Type-2 and 2bis inverters) is very efficient to minimize the shift as the threshold voltages decrease. The Type-3 buffer shows no shift at all at any dose for a 0V-input voltage during irradiation and the smallest shift (-0.1V after 2.3Mrad(Si)) for the worst case bias during irradiation. On the contrary, the "pull-up" configurations (Type-1 and 1bis inverters) lead to shifts of the transfer characteristics larger than the normal inverter for both input biases. Formulas (6-1) and (6-2) show that this occurs when ΔV_{thp} is larger than ΔV_{thn}, which is the case resulting from this irradiation.

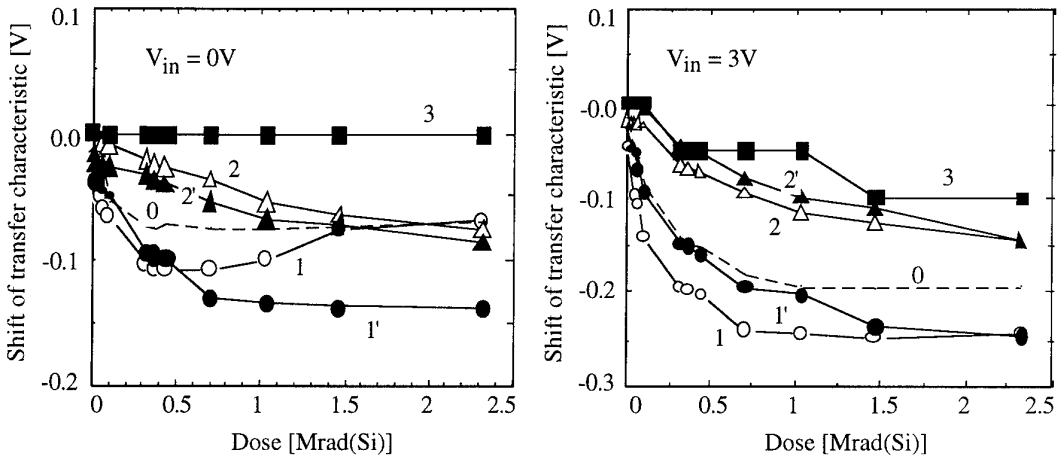

Figure 6.12: Shift of the transfer characteristic in GAA inverters as a function of dose. V_{dd} = 3V. On the left, V_{in} = 0V during the irradiation. On the right, V_{in} = 3V during the irradiation. 0: Classical, 1: Type-1, 1': Type-1bis, 2: Type-2, 2': Type-2bis, 3: Type-3 inverters.

3. Static RAM total-dose hardening

Static memories have a non destructive readout and retain data as long as the supply voltage is applied. Static RAMs are therefore inherently more robust against total-dose irradiation than dynamic RAMs which need the application of a periodic refresh. Many experiments have been carried out to evaluate the total-dose hardness of static RAMs

processed in various technologies, for example: bulk silicon [8,9], SOS [10,11] and SOI [12,13]. But there is a lack of general discussion about the design which has to be adopted in order to reach maximum hardness. Trying to provide a universal solution is of course utopian, but some theoretical considerations could usefully guide the designer. After briefly looking at the peripheral circuits, which are not the most critical parts of the SRAM, the analysis focuses on the memory cell. It is generally not possible to introduce compensation circuits such as those depicted in Figure 6.3 in each memory cell, because this would lead to prohibitive chip sizing. The stability upon total-dose irradiation of the classical CMOS six-transistor cell is then theoretically explored. An analytical expression for the stability of the basic cross-coupled inverters as a function of threshold voltage shifts is first derived explicitly. Next, the limits of proper write- and non destructive read-operations in the case of n- and p-channel access device designs are studied with the aid of numerical and graphical methods. Finally, the total-dose performance of 1k SRAM realized using the very promising GAA technology is presented up to 85Mrad(Si).

3.1. Peripheral circuits

In an SRAM two decoders perform the horizontal selection of one column of cells, and the vertical selection of one row of cells, one write and/or one read circuit for each access. The input is common for all write circuits while several read circuits feed a single output buffer. The information transits along the bit lines of a row (BL and BLB) from the input to the cell and from the cell to the output, while the selection of the cell (column) is piloted by the word line (WL) (Figure 6.16).

Increased n-leakage and reduced p-drive lead to the following fundamental design option choices for the different basic blocks.

• Decoders are realized by combining fully static CMOS AND gates which are the most robust logic gates against total-dose irradiation.

• The write driver can either be of the "transfer gate" type or the "C^2MOS gate" type as shown in Figure 6.13. Some authors consider that the bias under irradiation is less severe for C^2MOS circuits so that threshold voltage shifts are less pronounced [14]. But since the series combination of p-channel devices should be avoided, we have chosen the complementary "transfer gate" approach.

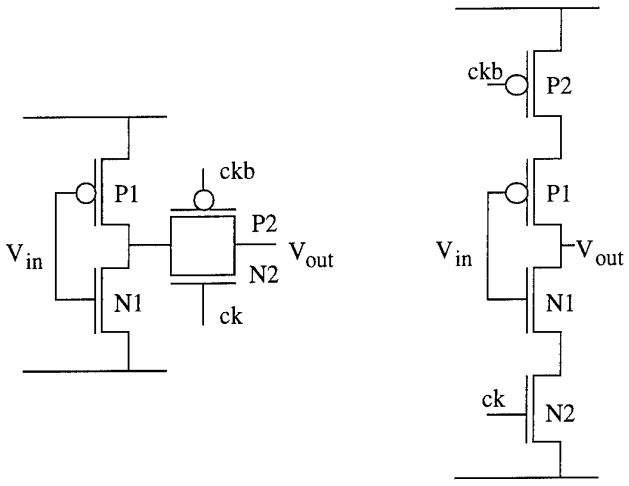

Figure 6.13: Write driver: transfer gate on the left and C^2MOS circuit on the right.

• The read circuit consists in a differential sense amplifier. Full CMOS solutions such as the single-ended design (Figure 6.14, left) are generally adopted. Active circuits which provide a positive feedback to the read operation (Figure 6.14, right) are known to increase speed but they are also less radiation-hard since they introduce a direct leakage path between the bit lines and ground. The radiation hardness of CMOS design is, of course, enhanced if the size of the p-channels devices (P1, P2) largely exceeds the size of the n-channel transistors (N1, N2). In order to keep both area and internal capacitance within tolerable limits, the p-type current mirror can be shared by all read circuits. The current source of the amplifier is made of a simple n-channel transistor (N3) driven by the horizontal decoder (ck). Choosing the appropriate size for this source transistor is a difficult task. Indeed, a large size enhances speed and also decreases the on-resistance which better preserves the output dynamic as soon as leakage currents appear. But, on the other hand, the isolation between the different read circuits (that feed the same output buffer) relies on the correct turn-off state of this source transistor. From this viewpoint, a small size is preferable to limit leakage and parasitic mutual interactions.

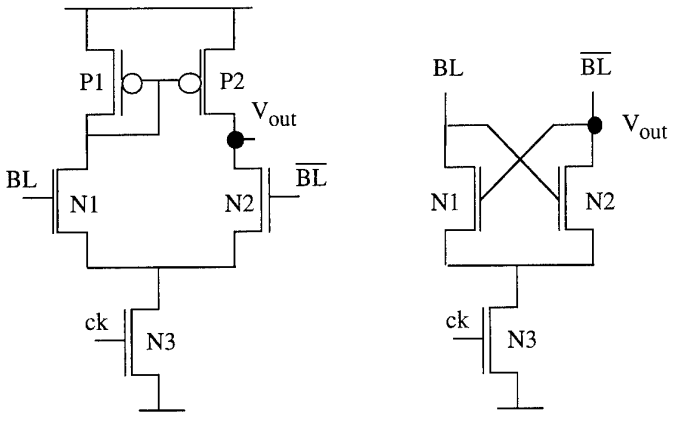

Figure 6.14: Differential sense amplifier: full CMOS single ended design on the left and active feedback design on the right.

• A precharge cycle is required to equalize the voltages of the bit lines and to avoid an undesirable switching of the cell at the beginning the read operation. During the precharge cycle, the bit lines are pulled high, the word lines are pulled low, and all nodes in the differential sense amplifier and write driver are biased symmetrically as usually recommended [4]. Precharge circuits are formed by p-channel transistors in order to avoid leakage. Between the two possible designs presented in Figure 6.15, the stable circuit (left) is chosen. Indeed, the cross-coupled (meta-stable) solution (right) amplifies any voltage difference appearing on the bit lines as soon as the equalizer transistor (P3) is turned off. If this action is interesting to accelerate the read operation, the feedback also enhances any undesirable imbalance (due to parasitic leakage currents) occurring before the access devices of the memory cell are completely turned on.

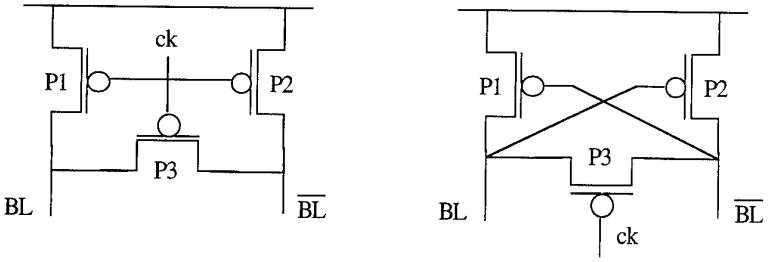

Figure 6.15: P-channel precharge circuit: stable version on the left and cross-coupled (meta-stable) solution on the right.

The above recommendations generally reduce speed and increase area but probably provide the best tolerance against negative threshold voltage shifts. If further speed and compactness reductions are allowed, compensation circuits (Figure 6.3) could be inserted in read and/or write circuits if necessary.

3.2. Static memory cells

On the contrary to peripheral circuits, memory cells are repeated a huge number of times. They should stay as compact as possible and cannot be hardened so easily by introducing additional transistors. They are, therefore, the weakest elements of SRAMs. Although static-noise margin analyses of the cell as a function of supply voltage, device sizes and mismatches are widely available [15,16,17], nothing has been performed, to our knowledge, about total-dose. A theoretical analysis of the intrinsic total-dose tolerance of CMOS static cells is therefore explicitly derived in the following.

The memory cell, depicted in Figure 6.16 with read, write and precharge circuits, consists of two cross-coupled inverters (P1-N1, P2-N2) accessed through a pair of transistors A1 and A2. Usually n-channel transfer transistors are chosen to benefit from their higher current drive capability. In this case, transistors N1 and N2 should be considered as driver devices and transistors P1 and P2 as loads. The reverse situation occurs with a p-channel access. Generally, the size of the load devices is kept as small as possible while the size of driver devices determines the speed.

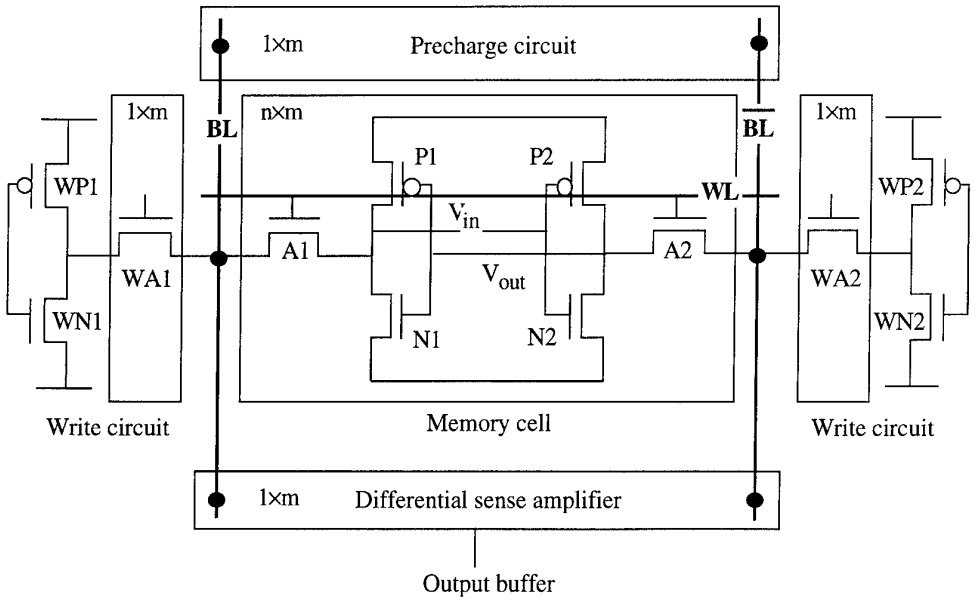

Figure 6.16: Schematic of the CMOS SRAM. The width to length ratio of the different transistors are: N: 4, P: 1, A: 1, WA: 3, WN: 4, WP: 12.

3.2.1. Isolated cross-coupled inverters

The stability of the two identical cross-coupled CMOS inverters may be graphically visualized in Figure 6.17 showing the normal (N) and mirrored (M) transfer characteristics before (curves Na-Ma) and after (curves Nb-Mb) a 1V-negative shift of both threshold voltages. In the following, the supply voltage is assumed to be 3V.

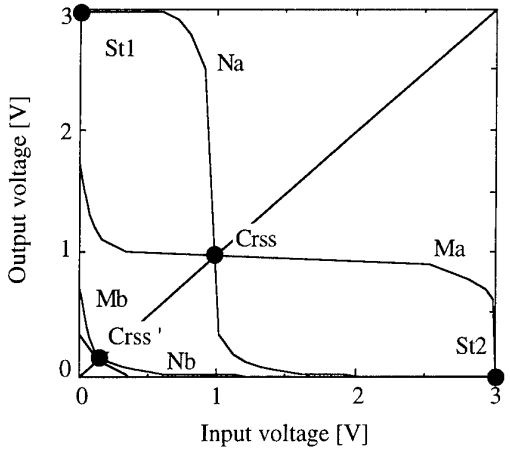

Figure 6.17: Normal and mirrored transfer characteristics of a CMOS inverter with $(W/L)_N = 4$, $(W/L)_P = 1$, $V_{dd} = 3V$ and a) $V_{thn} = 0.55V$, $V_{thp} = -0.673V$, b) $V_{thn} = 0.55V-\Delta V_{th}$, $V_{thp} = -0.673V-\Delta V_{th}$, $\Delta V_{th} = 1.0V$.

The normal N and mirrored M transfer curves intersect at a stable point (such as St1, St2) if $|\partial N/\partial V_{in}| \leq |\partial M/\partial V_{in}|$, while an unstable point (such as Crss) is obtained if $|\partial N/\partial V_{in}| \geq |\partial M/\partial V_{in}|$. Before irradiation (curves Ma-Na), the memory cell is able to store two different stable states (St1 and St2). When V_{thn} decreases below zero, the high logic level degrades and moves away from the supply voltage V_{dd}, but the two stable

states still exist. For further V_{th} decrease (curves Mb-Nb), the crossover point (Crss ') of the transfer characteristics becomes the only stable point which implies the loss of the information stored in the cell.

Applying one of the several equivalent stability criteria [17], and assuming two identical inverters, the logic operates properly (the cell has still two different stable states) as long as:

$$\left| \left(\frac{\partial N}{\partial V_{in}} \right)_{V_{in}=V_{out}} \right| > 1$$

with $V_{in} = V_{out} = V^*$ being the crossover point of the normal and mirrored curves. Since the data retention capability of the two cross-coupled inverters vanishes out at a sufficient negative V_{thn}, we assume that P1(P2) and N1(N2) operates in the saturated and linear regions respectively. This has been numerically verified. Since the currents flowing through P1 and N1 are the same, it comes, with the usual first order approximation for the drain currents (the body factor *n* is equal to unity in GAA devices):

$$\beta_n \left[(V_{in} - V_{thn}) V_{out} - \frac{V_{out}^2}{2} \right] = \beta_p \frac{\left[V_{dd} - |V_{thp}| - V_{in} \right]^2}{2} \qquad (6\text{-}3)$$

and, with $\alpha = \beta_n/\beta_p = \mu_n (W/L)_N / \left(\mu_p (W/L)_P \right)$,

$$V_{out} = (V_{in} - V_{thn}) \left\{ 1 - \sqrt{1 - \frac{\left(V_{dd} - |V_{thp}| - V_{in} \right)^2}{\alpha (V_{in} - V_{thn})^2}} \right\} \qquad (6\text{-}4)$$

Imposing that the slope $\partial V_{out}/\partial V_{in}$ of the transfer characteristic (6-4) is equal to -1 with $V_{in} = V^*$, it comes:

$$\frac{(1-\alpha)V^* - \left(V_{dd} - |V_{thp}| \right)}{(-\alpha V_{thn})} = -1 \qquad (6\text{-}5)$$

Rewriting (6-3) and (6-5) as a function of V^*, we finally have to solve:

$$\begin{cases} (\alpha - 1)V^{*2} + 2\left(V_{dd} - |V_{thp}| - \alpha V_{thn} \right) - \left(V_{dd} - |V_{thp}| \right)^2 = 0 \\ (1-\alpha)V^* = V_{dd} - |V_{thp}| + \alpha V_{thn} \end{cases}$$

which gives:

$$(V_{dd} - |V_{thp}|)^2 = 3\alpha (V_{thn})^2 + 2V_{thn} (V_{dd} - |V_{thp}|)$$

or equivalently, with $V_{thn} < 0$ and $V_{dd}+V_{thp} > 0$:

$$V_{dd} - |V_{thp}| = \left(1 - \sqrt{1+3\alpha} \right) V_{thn} \qquad (6\text{-}6)$$

Figure 6.18 depicts relationship (6-6) in the V_{thn}-$|V_{thp}|$ plane as a function of $(W/L)_P$ with $(W/L)_N = 4$ and $\mu_n/\mu_p = 2.3$. The linear failure curve separates the V_{thn}-$|V_{thp}|$ plane in two regions: data retention is possible in the left part, not in the right one. If V_{thn} is too negative, the information stored is lost. The minimum negative value of V_{thn} (before the possible rebound) mainly determines if the forbidden region is reached or not during irradiation. From this point of view, it is better to start with relatively low $|V_{thpo}|$ and high V_{thno}.

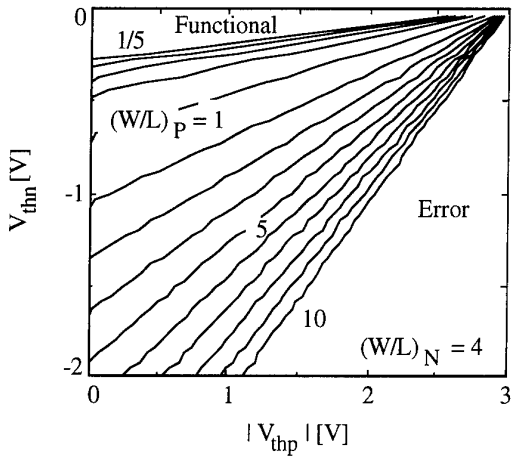

Figure 6.18: Failure boundary of the data retention in an isolated flip-flop, depicted in the V_{thn}-$|V_{thp}|$ plane, with $(W/L)_P$ as parameter and for $(W/L)_N = 4$. $V_{dd} = 3V$.

Finally, assuming that $V_{thn} = V_{thno}-\Delta V_{th}$ and $|V_{thp}| = |V_{thpo}|+\delta\Delta V_{th}$, the maximum allowed threshold voltage shift still giving two stable states is:

$$\Delta V_{th,max} = \frac{\left(V_{dd} - |V_{thpo}|\right) - \left(1 - \sqrt{1+3\alpha}\right)V_{thno}}{\delta - 1 + \sqrt{1+3\alpha}} \qquad (6\text{-}7)$$

With $\delta = 1$ (as experimentally observed with $V_G = 3V$ and 0V respectively for n- and p-channel devices during irradiation) and with $V_{dd} = 3V$, $V_{thno} = 0.55V$, $V_{thpo} = -0.67V$, $(W/L)_P = 1$ and $(W/L)_N = 4$ ($\alpha = 9.23$), $\Delta V_{th,max}$ is 0.88V which corresponds to $V_{thn} = -0.33V$.

As expected from (6-7) and Figure 6.18, the maximum allowed threshold voltage shift is a decreasing function of α. This means that an intrinsically higher radiation hardness is obtained when increasing the size of the load transistors (decreasing the size of driver devices is not recommended since it reduces the memory access speed). In this manner, inverters can tolerate important negative threshold voltage shifts up to several volts before loosing the information stored. Unfortunately, we will show that the read operation will drastically limit the total-dose performance before data retention failure arises.

3.2.2. The write operation

Before discussing the read operation, the write operation should be investigated because it determines the minimum size of the access devices to the cell. The write operation is performed differentially by forcing high and low voltages to a pair of bit lines

as sketched in Figure 6.19. We assume that, before the write operation, the cell internal voltages are V_{in} = 0 and V_{out} = V_{dd}. As a consequence, to reverse the cell state, transistors WP1, WA1, A1, A2, WA2 and WN2 must be turned on, while devices WN1 and WP2 (shown in Figure 6.16) are turned off. The macro cross-coupled inverters of the cell are therefore no longer symmetric, even if they are affected by the same threshold voltage shifts during irradiation: the left inverter is loaded through the access transistors by the pull-up device WP1, while the right inverter is loaded by the pull-down transistor WN2. Simple n-channel transistors WA1, WA2 replace the complementary pass gate of the write circuits for simplification.

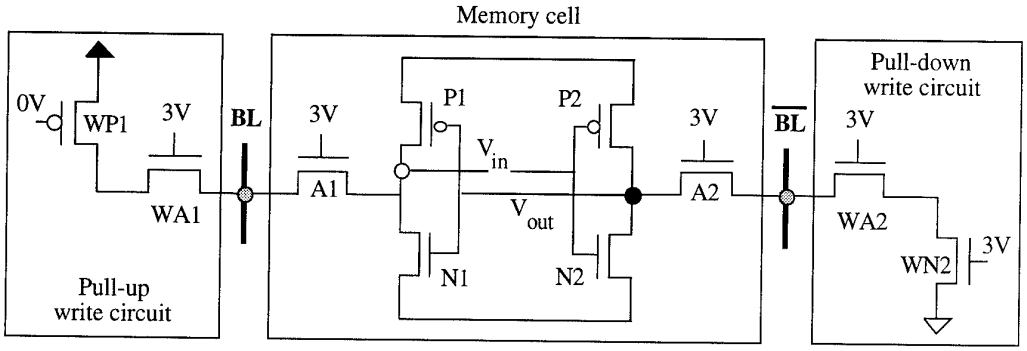

Figure 6.19: Schematic of the SRAM cell loading during the write operation.
The width-to-length ratio of the different transistors are: N: 4, P: 1, WA: 3*A, WN: 4, WP: 12.

The normal(mirrored) transfer characteristic of the right(left) asymmetrical macro inverters are shown in Figure 6.20. The transistor sizes are mentioned in the caption of Figure 6.19. Gate devices of the write circuit (WA1, WA2) are three times larger than the access devices of the cell (A1, A2). Before the write operation, the cell is in the stable state St1 (V_{in} = 0 and V_{out} = V_{dd}). At the beginning of the access, V_{out} drops to point A' and V_{in} slightly increases to point A". A' is the voltage at node V_{out} with transistors P2, A2, WA2 and WN2 in the on-state, with WP2 in the off-state and assuming N2 still completely turned off. In the same way, A" is the voltage at node V_{in} assuming that P1 is turned off. Figure 6.20 clearly shows that the write operation is mainly performed by the action of the pull-down circuit, the pull-up structure having a limited influence. The cell switches to the other state St2 provided that the width of the access transistors is sufficient, case represented in Figure 6.20 by curves Ma-Na obtained with $(W/L)_{A1,A2}$ = 1. If the size (or, more generally, the driving capability) of the access devices A1, A2 decreases, the wide gap between the two transfer curves shrinks and finally the curves intersect at a new intermediate stable state St3 as illustrated by curves Mb-Nb obtained with $(W/L)_{A1,A2}$ = 0.35. In this case, the switching stops at stable state St3 and the system never reaches stable state St2: the write operation fails.

It is impossible to analytically compute the expression of the minimum size required for the access devices A1, A2 in order to obtain a correct write operation. The simple criteria mentioned previously for the two symmetrical isolated inverters is indeed useless, since the two macro cross-coupled structures are now asymmetrical. A more general condition specifying the tangency of the normal and mirrored transfer characteristics leads to search a double root of a fourth-order equation. This problem has no analytical solution. Moreover, the regime of the different transistors during the switching is not

clearly identified and may vary with transistor sizes. Therefore, computations will be performed numerically. Three possibilities exist for each transistor of Figure 6.19: the off-state, and the on-state in linear or saturation operation. We again use a first-order model for the drain current in linear and saturated regimes and the current is ideally supposed to be zero as soon as $V_G < V_{thn}$ or $V_G > V_{dd}+V_{thp}$. The convergence of the global system for each value of V_{in} is obtained using the Newton-Raphson iterative method. The detection of stable and unstable states is performed by means of a very simple definition of the static noise margin SNM. The SNM is indeed computed as the horizontal difference between the two transfer curves as shown in Figure 6.20: SNM = $M(V_{out})$-$N(V_{out})$. A crossover point of the two curves is unstable if, at increasing V_{out}, the SNM from positive becomes negative, while a transition from negative to positive values of the SNM provides a stable point. As a consequence, the write operation is possible if the SNM remains positive from $V_{out} = 0$ up to $V_{out} = V_{dd}$, since, in this case, the only intersection point of the two curves is stable state St2.

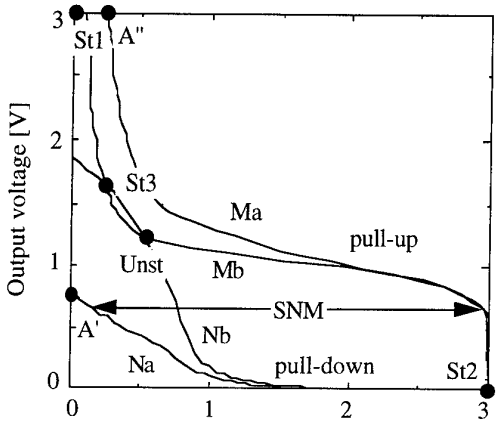

Figure 6.20: Normal and mirrored transfer characteristics of the right and left loaded inverters during the write operation with $(W/L)_N = 4$; $(W/L)_P = 1$; $V_{dd} = 3V$; and a) $(W/L)_A = 1$, b) $(W/L)_A = 0.35$. ($V_{thn} = 0.55V$; $V_{thp} = -0.673V$).

Figure 6.21 shows the write operation boundary in the V_{thn}-$|V_{thp}|$ plane as a function of the pair $(W/L)_P$ - $(W/L)_A$ with $(W/L)_N = 4$. The plane is again split in two regions: in the upper part, the write operation fails, in the lower part, the write operation succeeds. The error region is found in the upper left corner since the write operation is more difficult as V_{thn} increases, when the driving capability of the n-channel access devices drops. The boundary also presents a positive slope with respect to $|V_{thp}|$ which indicates that the write operation is easier with weaker load transistors (larger $|V_{thp}|$). To extend the functional area and push the boundary towards the upper left corner, which allows to choose a large positive prerad value of V_{thn} or to sustain a strong positive rebound of V_{thn} upon irradiation, we may either increase $(W/L)_A$ keeping $(W/L)_P$ constant (solid curves) or decrease $(W/L)_P$ at constant $(W/L)_A$ (dashed lines). This is opposed to the increase of $(W/L)_P$ recommended to harden isolated flip-flops against large negative V_{thn} shifts.

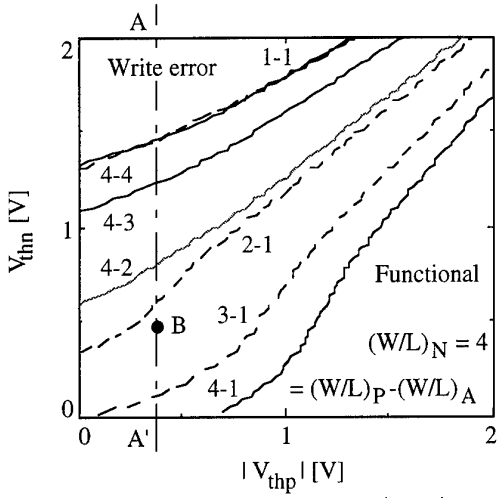

Figure 6.21: Evolution of the write failure boundary in the V_{thn}-$|V_{thp}|$ plane as a function of the pair $(W/L)_P$-$(W/L)_A$ with $(W/L)_N = 4$. Solid curves: $(W/L)_A$ is swept from 1 to 4 and $(W/L)_P = 4$. Dashed lines: $(W/L)_P$ is swept from 1 to 4, $(W/L)_A = 1$. $V_{dd} = 3V$.

To further highlight this last point, we have plotted in Figure 6.22 the minimum size of the access devices so that the write operation is possible at point B of Figure 6.20 as a function of $(W/L)_P$. The larger $(W/L)_P$, the larger $(W/L)_A$. The different curves are obtained moving point B in the worst case situation where point B translates vertically along section AA' : $|V_{thp}|$ is kept constant at 0.4V and V_{thn} is swept from 0V to 2V by steps of 0.2V. When V_{thn} is smaller than 1V, $(W/L)_A$ follows $(W/L)_P$ in a sub-linear way. The cell area grows therefore less rapidly than $(W/L)_P^2$. With V_{thn} above 1V, the write operation would require an unacceptable cell area for large values of $(W/L)_P$. Hence, $(W/L)_P$ cannot be increased to enhance the data retention hardness against large negative V_{thn} shifts when a subsequent large positive rebound of V_{thn} is of concern.

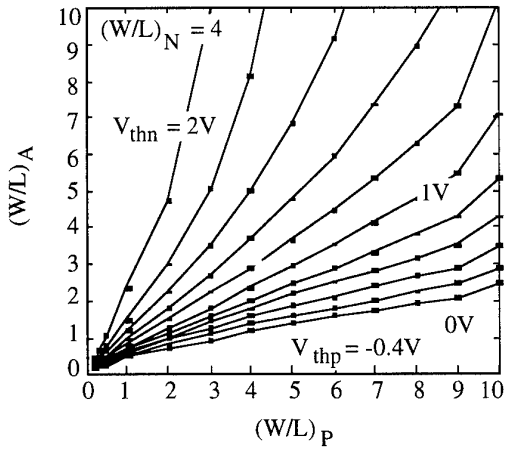

Figure 6.22: Minimum size of the access transistor as a function of the size of the load device with V_{thn} as parameter swept from 0V to 2V by 0.2V steps. $|V_{thp}| = 0.4V$ and $(W/L)_N = 1$. $V_{dd} = 3V$.

The write operation generally will not fail upon radiation exposure since the path followed in the V_{thn}-$|V_{thp}|$ plane during irradiation first moves away from the boundary with decreasing V_{thn}. As shown in Figure 6.21, the slope of the write boundary tends to unity for large values of $|V_{thp}|$. Therefore, a write failure could eventually occur at very

high dose, provided that V_{thn} rebounds with a ratio $\Delta V_{thn}/\Delta|V_{thp}|$ much larger than unity.

3.2.3. The read operation

The information stored in a memory cell has to be read non destructively. Theoretically, a correct read operation occurs provided that the bit lines are both precharged at the same high level before the read access [16]. However, assuming a perfect precharge cycle, leakage currents through the access devices of adjacent cells could lead to reverse the cell state during the read operation. Furthermore, the reduced driving capability of precharge devices and increased leakage currents could lead to an incomplete and/or not equal precharge of the bit lines. This imperfect precharge cycle may lead to switch the cell state at the beginning of the read access.

3.2.3.1. Leakage currents during the read operation

During the read operation, leakage occurs through the turned-off access transistors of the other cells sharing the same bit lines and through the turned-off access device of the write drivers. The full CMOS single-ended differential read amplifier has been chosen because it is free of leakage path between the bit lines and ground. During the whole read access time, the cross-coupled inverters are loaded by the "on" access transistors of the cell (A1,A2) cascaded by the "off" gate devices (AA1, AA2) replacing other cells and write circuits as shown in Figure 6.23.

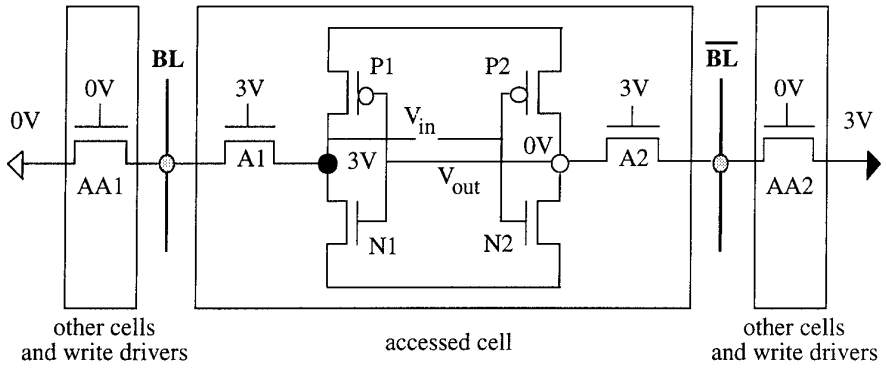

Figure 6.23: Schematic of the SRAM cell loading during the read operation.
The width-to-length ratio of the different transistors are: N: 4, P: 1, WA: 3*A, WN: 4, WP: 12.

With the accessed cell initially in "state-1" (V_{in} = 3V and V_{out} = 0V), an adverse action of devices AA1 and AA2 occurs if AA1 is connected to ground and AA2 is connected to V_{dd} (Figure 6.23). The size of the transistors AA1 and AA2 should then be computed as the difference between the number of cells in "state-0" and the number of cells in "state-1". Obviously, all the patterns stored in the memory do not present the same irradiation sensitivity. The worst case situation appears when the accessed cell is in a given state while all other cells belonging to the same row contain the opposite data (for example, the "walking diagonal" pattern). Considering this worst-case situation, the size of transistors AA1 and AA2 strongly depends on the memory architecture and certainly

increases with memory size. The transfer characteristics of the two cross-coupled loaded inverters are computed numerically for negative n-threshold voltages. The read operation is non destructive if two stable states St1, St2 are observed as in Figure 6.17. In other words, the read operation fails if it acts as a write operation, detected, as previously, by the absence of negative values of the SNM between 0V and V_{dd}.

Choosing the minimum size for the access devices such that the write operation is possible with V_{thn} = 0.6V and V_{thp} = -0.6V before irradiation (which helps the isolation between memory cells), and introducing AA1 = AA2 = 2^5-1 "off" gate transistors (as in a square 1kbit memory), we obtain the read error boundaries of Figure 6.24 with $(W/L)_P$ as parameter (curves "L0.2", "L1" and "L5" with $(W/L)_P$ = 0.2, 1 and 5, respectively). The V_{thn}-$|V_{thp}|$ plane is again separated into two regions. The read operation is correct in the upper part. Leakage currents essentially tend to destroy the high logic state of the accessed cell because the action of the pull-down side is stronger than the action of the pull-up side as for the write operation. As a result, the read operation is reinforced by stronger load devices and the boundary between the "functional" and "error" regions exhibits a positive slope as a function of $|V_{thp}|$. Also, the functional area slightly extends as $(W/L)_P$ increases. Previous results from (6-3) giving the hardness of isolated cross-coupled inverters are also shown in Figure 6.24 (curves "I0.2", "I1" and "I5" with $(W/L)_P$ = 0.2, 1 and 5, respectively). It is quite clear that the "read error" related to curves "L" (inversion of the information stored in the cell during the read access) occurs far before the "retention error" related to curves "I" (equality of high and low voltages in the isolated cell implying data loss).

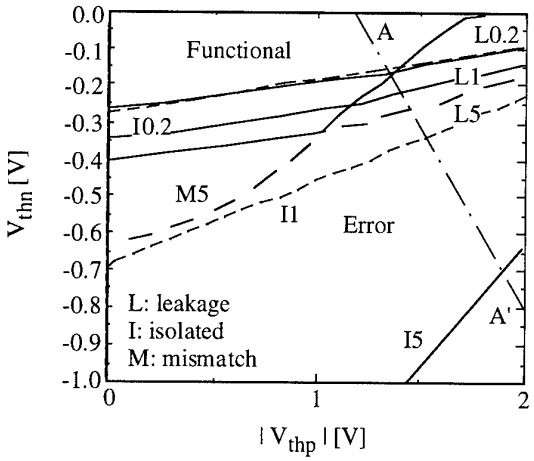

Figure 6.24: Evolution of the different read failure boundaries in the V_{thn}-$|V_{thp}|$ plane with $(W/L)_N$ = 4, minimum $(W/L)_A$ and V_{dd} = 3V:
I0.2, I1, I5 : Retention failure of Isolated flip-flops with $(W/L)_P$ = 0.2, 1 and 5, respectively.
L0.2, L1, L5: Leakage currents failure with $(W/L)_P$ = 0.2, 1 and 5, respectively and with 2^5-1 "off" gate devices.
M5: Mismatch failure with $(W/L)_P$ = 5: one bit line at V_{dd} and the other at 80% of V_{dd}.

Along section AA' in Figure 6.24, the threshold voltage shifts of n- and p-type devices are identical (V_{thn} = 0.6-ΔV_{th}, V_{thp} = -0.6-ΔV_{th}). This section fits experimental data before the rebound of V_{thn} presented in Chapter V. Figure 6.25 (left) depicts the read operation limit as a function of $(W/L)_P$ along this section with the size of transistors AA1 and AA2 as parameter (curves "La", "Lb", "Lc": with 2^3-1, 2^5-1, 2^{10}-1 "off" gate

devices, respectively). With few memory cells sharing the same bit lines (curve "La"), an increase of $(W/L)_P$ improves the radiation hardness. Nevertheless, curve "La" cannot reach the performance expected from the two isolated cross-coupled inverters (curve "I"). In larger memories (curve "Lc"), increasing $(W/L)_P$ above 1 has no influence, the read failure boundary being nearly vertical. The explanation is the following: the read operation is hardened when the write operation is underprivileged, which occurs with stronger load devices. But, since the write operation must still be feasible, using larger load devices requires larger access devices which, in turn, increases the sensitivity of the read operation and increases leakage from adjacent cells. The net result of these competitive trends, is an improvement of the read hardness with increasing load size in small memories where the influence of leakage currents is weak. Unfortunately, virtually no enhancement can be achieved in large memories.

3.2.3.2. The precharge

The second limitation of the read operation is linked to the precharge levels of the bit lines. Clocked precharge transistors are p-channels in order to suppress one possible source of leakage during the read operation. Unfortunately, the precharge slows down upon irradiation due to the negative V_{thp} shift. If the operating frequency is unchanged, the final precharge level could decrease with dose. On the other hand, a mismatch between the precharge levels of the bit lines is also detrimental to the read operation. Such a mismatch, dependent on the clock frequency, could occur if the threshold voltage shifts of precharge devices are not identical as a consequence of the non-uniform bias present at the different nodes during irradiation. Furthermore, leakage currents that oppose the precharge are not necessarily identical for the two bit lines, which is another possible cause of mismatch.

To investigate the sensitivity of the memory cell design to the precharge conditions, we connect the bit lines to voltage sources representing their respective voltages at the beginning of the read operation, and we turn on the cell access devices. We check, owing to the numerically computed SNM between the normal and mirrored transfer characteristics, if two distinct stable points exist. If not, the information is destroyed. The procedure yields very conservative results since, in practice, the bit lines are capacitive loads which deliver less current than voltage sources. In Figure 6.25 (right), curve "C" indicates the threshold voltage shift necessary to obtain a failure with both bit lines at 50% of V_{dd}. This curve represents the sensitivity of the read operation to the completion of the precharge. Curve "C" moves to the left as the precharge level increases demonstrating the improvement provided by a precharge to a higher level especially when $(W/L)_P$ is close to unity. Curves "Ma" and "Mb" represent the read failure due to a mismatch between the two precharge levels: one bit line is held at V_{dd}, the other is maintained at 80% and 60% of V_{dd} for "Ma" and "Mb", respectively. Mismatch errors are generally more critical than completion errors (errors due to precharge partial completion), because a mismatch tries to switch the cell state while symmetrical partial completion simply tends to equalize both cell internal voltages.

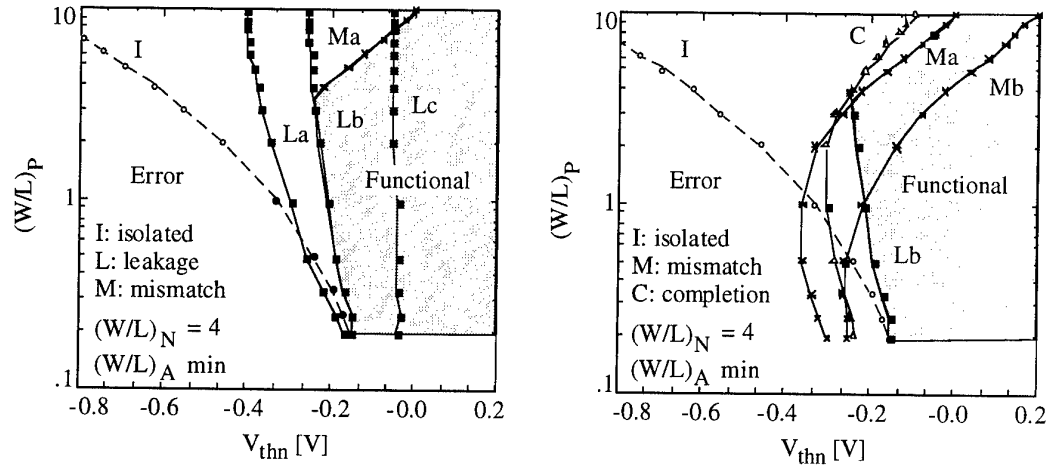

Figure 6.25: Failure boundaries of the read operation as a function of $(W/L)_P$ with $V_{thn} = 0.6V-\Delta V_t$, $V_{thp} = -0.6V-\Delta V_t$, $(W/L)_N = 4$, minimum $(W/L)_A$ and $V_{dd} = 3V$:
I : Retention failure of **I**solated flip-flops.
L: **L**eakage currents failure: 2^3-1 (La), 2^5-1 (Lb), and 2^{10}-1 (Lc) "off" gate devices.
C: **C**ompletion failure: both bit lines precharged at 50% of V_{dd}.
M: **M**ismatch failure: one bit line at V_{dd} and the other at 80% (Ma) and 60% (Mb) of V_{dd}.

Figure 6.25 (right) also shows that increasing $(W/L)_P$ above 1 increases the sensitivity to mismatch errors due to the wider access transistors required by the write operation. The problem is that mismatch errors become the limiting factor of radiation hardness for large $(W/L)_P$ values as soon as "M-curves" are situated to the right of "L-curves". This is also clearly observed in Figure 6.24 where curve "M5", corresponding to mismatch errors, is above curve "L5", corresponding to the leakage currents action, for $|V_{thp}| > 1V$. Therefore, increasing $(W/L)_P$, which seemed up to now to be globally favorable to the radiation hardness (or at least neutral), now clearly appears to be detrimental in some situations.

3.2.4. Choice of an appropriate n-gated design

We know that the tolerance to negative threshold voltage shifts of two isolated cross-coupled inverters is improved when the size of the load devices $(W/L)_P$ is increased. This implies a subsequent increase of the access device size $(W/L)_A$ so that the write operation remains possible. Fortunately, the write operation does not seem to become critical upon irradiation exposure. Now, as far as the read operation is concerned, an increase of $(W/L)_P$ improves the hardness but the subsequent increase of $(W/L)_A$ required by the write operation, has the opposite effect. Therefore, there is an optimum value for $(W/L)_P$ that depends on the adverse action of leakage currents or precharge mismatch. This optimum can be found graphically. The shaded area of left and right parts of Figure 6.25 for instance, represents the functional region for a square 1kbit memory tolerating 80% mismatch on the precharge levels. The failure boundary due to the adverse action of leakage currents (L-errors) is represented by curve "Lb" while the failure boundary due to the mismatch between the precharge levels (M-errors) is curve "Ma". Above $(W/L)_P = 1$, the hardness to L-errors and M-errors respectively increases and decreases with larger $(W/L)_P$. The optimum value of $(W/L)_P$, giving the maximum negative threshold voltage that the memory could sustained, is therefore obtained at the intersection of curves "Lb"

and "Ma": $(W/L)_P$ optimum is around 3 and ensures a correct memory operation down to V_{thn} = -0.2V. If a larger mismatch is susceptible to occur (curve "Mb"), the optimum shifts towards weaker values of $(W/L)_P$ and produces a less negative maximum threshold voltage shift. The total-dose hardness of larger memories (curve "Lc" for a square 1Mbit structure) cannot be significantly improved by increasing $(W/L)_P$ above usual values (close to unity) so that their operation is restricted to nearly strictly positive V_{thn} values.

3.2.5. Cells with p-type access transistors

The goal is now to investigate whether cells with p-type gate devices provide an elegant solution against radiative environments when V_{thn} becomes too negative. Since $|V_{thp}|$ increases steadily with dose, p-channel devices do not risk leakage currents but the reduced driving capability of pass transistors is the limiting factor.

During the write operation, the loading scheme of the cross-coupled inverters is depicted in Figure 6.19 where n-type access devices (A1, A2, WA1, WA2) should be replaced by p-channel transistors. Figure 6.26 shows, in the V_{thn}-$|V_{thp}|$ plane, the numerical computation of the boundary for correct write operation (series of curves "A" and "N"): writing is only possible in the left region. The internal operation of the cell is reversed compared to the n-type access case, with p-type transistors as drivers and n-channel devices as loads. Therefore, the write boundaries of Figure 6.26 may be obtained from Figure 6.21 by means of a vertical flip around the V_{thn}-$|V_{thp}|$ axis. The boundary looks like a hyperbola with an asymptote for large values of $|V_{thp}|$. As previously, the region where the write operation is possible enlarges with increasing size of pass transistors at constant $(W/L)_N$ (curves A1 to A4, with $(W/L)_A$ = 1 to 4 and $(W/L)_N$ = 1) or with decreasing size of load devices and unchanged $(W/L)_A$ (curves N1 to N3, with $(W/L)_N$ = 1, 1/2, 1/3 and $(W/L)_A$ = 1). The tremendous advantage compared to the n-gate case is that here a reduction of the load device size also decreases $\alpha \div (W/L)_N/(W/L)_P$ and consequently improves the radiation hardness of the isolated cross-coupled inverters to negative V_{thn} shifts as shown in (6-7). The disadvantage, on the other hand, is that the operating point approaches the write failure boundary during irradiation so that the cell sizing must be chosen for threshold voltages corresponding to the maximum dose.

Next, it will be shown that the read operation does not become critical upon radiation exposure and is not strongly also altered by decreasing the size of n-channels load devices. The read operation is only sensitive to the precharge levels (because p-channel access transistors avoid leakage currents between adjacent cells). The bit lines are pre-discharged at the ground voltage through n-channel transistors (which have to be very small so that their leakage currents do not disturb the read and write operations). Curves "M" in Figure 6.26 depict the failure due to a 20% mismatch between the bit line levels at the beginning of the read operation (one bit line at 0V and the other bit line at 0.6V with V_{dd} = 3V). Curve "M1" is obtained with $(W/L)_N$ = 1, $(W/L)_A$ = 1 as curve "A1-N1", while curves "MA2", "MN2", with $(W/L)_N$ = 1, $(W/L)_A$ = 2 and $(W/L)_N$ = 1/2, $(W/L)_A$ = 1, correspond to curves "A2", "N2", respectively. Wider access transistors always degrade the sensitivity of the read operation to precharge levels (curve "MA2"). Hence, the best way to extend the functional area of the write operation, without nearly affecting

the read operation, is to reduce the size of the load devices (curve "MN2"). We have checked that, for negative V_{thn} values, the read operation is still possible, at least as long as $|V_{thp}| < 2V$. For $V_{thn} < 0$, the proper memory operation is therefore theoretically only limited by the retention capability of the isolated cross-coupled inverters.

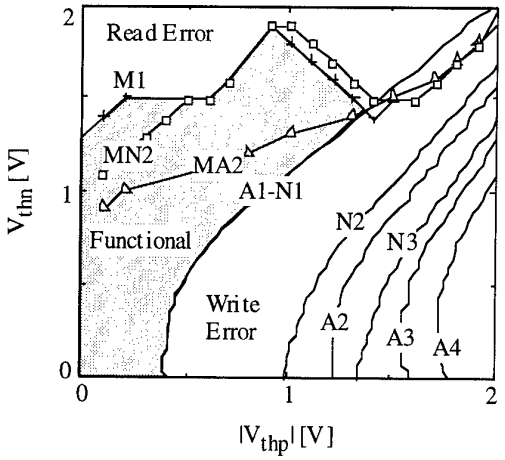

Figure 6.26: Evolution of the failure boundaries for a p-type gated cell in the V_{thn}-$|V_{thp}|$ plane as a function of the pair $(W/L)_N$-$(W/L)_A$ with $(W/L)_P = 1$ and $V_{dd} = 3V$:
A1 to A4: write boundary when $(W/L)_A$ is swept from 1 to 4, with $(W/L)_N = 1$
N1 to N3: write boundary when $(W/L)_N$ is respectively 1, 1/2, and 1/3 with $(W/L)_A = 1$
P1, PA2, PN2: read boundary with one bit line at 0V and the other at 0.6V at the beginning of the read access with the parameter corresponding to curves A1-N1, A2 and N2, respectively.
The shaded area is the functional region for $(W/L)_N = 1$, $(W/L)_A = 1$ and $(W/L)_P = 1$.

3.2.6. Comparison between n- and p-type access designs

The total-dose failure of the n-channel pass transistor cell design, due to destructive read operation, appears as soon as very small negative V_{thn} values are reached. Access devices no longer correctly isolate the different cells and leakage currents prevent any information storage. This limit can be slightly postponed by increasing $(W/L)_P$ with reduced efficiency when an increasing number of cells share the same bit lines. The increase of $(W/L)_P$ is also limited by precharge mismatch errors that become responsible for the failure point at large $(W/L)_P$. Furthermore, increasing $(W/L)_P$ requires a larger cell area which roughly increases like $(W/L)_P^2$. The write operation does not become critical provided that, when V_{thn} rebounds, its growing rate does not strongly exceed the increasing rate of $|V_{thp}|$.

The p-channel access device cell design becomes interesting if the goal is to sustain very large negative V_{thn} values ($V_{thn} < -0.2V$). Leakage currents are almost eliminated and the hardness of two isolated cross-coupled inverters could theoretically be reached. Correct memory operation up to the highest dose is obtained provided that the write operation is possible after irradiation: the cell sizing must ensure a sufficient driving capability of the access devices compared to the load and driver transistors for the maximum p-type threshold voltage shift. The disadvantage of the p-channel access design is that, at comparable cell area, the circuit speed is reduced by at least a factor μ_n/μ_p compared to n-type gated circuits. The speed reduction is generally enhanced after irradiation as illustrated by the following example. Choosing $(W/L)_P = 1$, $(W/L)_N = 4$,

$(W/L)_A = 1$ for the n-type gated cell and $(W/L)_P = 2$, $(W/L)_N = 0.66$, $(W/L)_A = 3.8$ for the p-type access case, the total cell area is approximately the same in both cases. Before irradiation ($V_{thn} = 0.6V$, $V_{thp} = -0.6V$), Spice simulations show that the n-type access cell discharges the 1pF-capacitance of the bit line down to 10% of V_{dd} ($V_{dd} = 3V$) within 18ns while the p-type cell needs 27ns to charge the bit line up to 90% of V_{dd}. The p-type cell is therefore 1.5 times slower. After irradiation, assuming 0.8V-negative threshold voltage shifts ($V_{thn} = -0.2V$, $V_{thp} = -1.4V$), the access times of n- and p-type access designs are in a ratio of 4, being respectively equal to 12ns and 47ns.

In conclusion, it seems that the classical cell design cannot be improved significantly against irradiation-induced leakage currents in SOI without introducing very large area and/or speed performance penalty. The radiation hardness therefore entirely relies on the choice of a proper technology capable to maintain V_{thn} above 0V.

3.3. Experimental performance of a 1k GAA SRAM

Since design-hardening techniques are not very efficient, one needs to demonstrate that sufficient total-dose hardness could be achieved using classical unhardened designs and an appropriate technology. This has been done by showing that a standard 1k SRAM realized in the GAA technology can successfully sustain 85Mrad(Si) irradiation.

The size of the driver, load and n-channel access devices of the memory cells are respectively $(W/L)_N = 4$, $(W/L)_P = 1$ and $(W/L)_A = 1$. The large drive transistor should ensure good speed performance. In GAA layouts, square devices (W/L = 1) occupy the smallest area because W/L >(<) 1 would require the parallel(series) combination of different transistors. With $(W/L)_P = 1$, the load device is hence kept as small as possible as in standard designs. This choice also nearly corresponds to the maximum hardness of the read operation that could be achieved by proper design (Figure 6.25). The access device size is also minimized to reduce the cell area. This limits the parasitic mutual interactions between cells due to leakage currents but degrades speed. Cells are arranged in a 32×32 array. In the middle of the polysilicon Word Line, a buffer of CMOS inverters refresh the running signal. Peripheral circuits that benefit from the largest stability upon irradiation are adopted: horizontal and vertical decoders are formed by a cascade of a 3-input NAND gates and the read circuits are made of single-ended CMOS differential current-mirror sense amplifiers (Figure 6.14, left) that all feed a three-stage CMOS output buffer. The write drivers are of complementary gate type (Figure 6.13, left) and the precharge is performed through simply clocked p-channel transistors (Figure 6.15, left). No compensation circuits such as those presented in Figure 6.3 are used. Figures 6.27 and 6.28 show the block diagram and the layout of the chip, respectively.

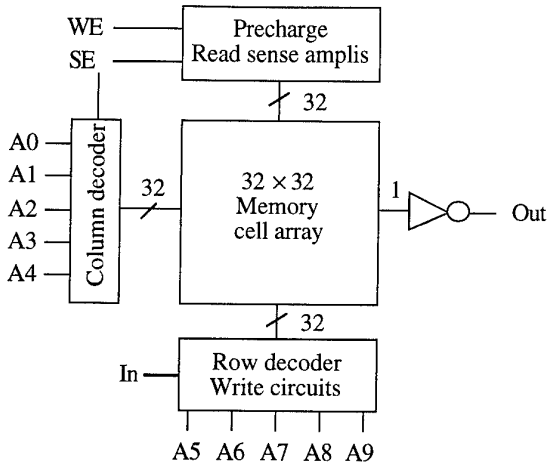

Figure 6.27: Block diagram of the 1k GAA SRAM. Pin names:

A0-A9	:	Input addresses
In	:	Input
Out	:	Output
SE	:	Select Enable
WE	:	Write Enable

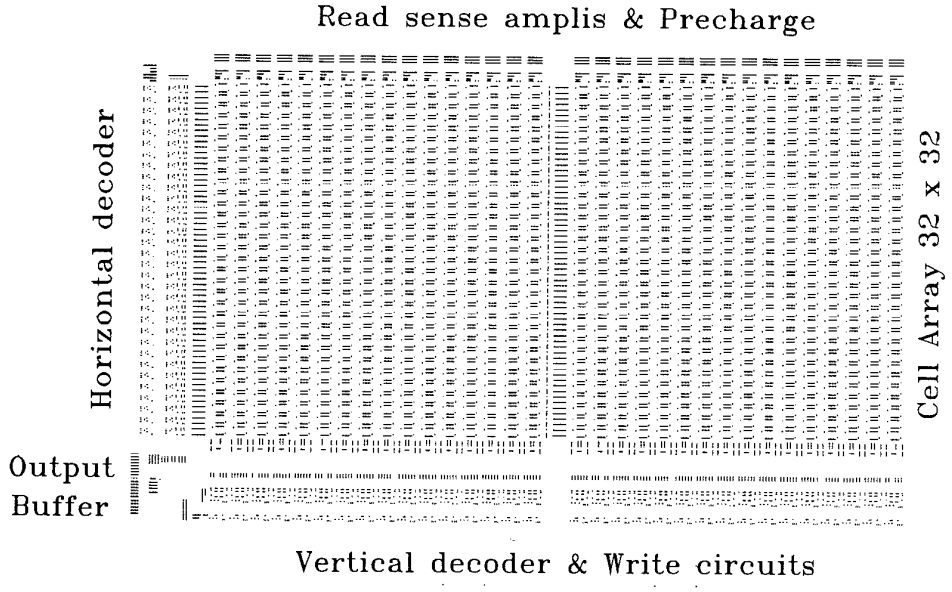

Figure 6.28: Layout of the 1k GAA SRAM, cavity layer. Chip size: 2.85mm × 4mm

The characteristics of the design and measured performance before irradiation are summarized in Table 6.2. The relatively poor compactness is due to the very conservative GAA layout rules (Figure 1.8). The access time (150ns) and Minimum Write Pulse (100ns) are very acceptable considering the high parasitic capacitances and the important source/drain series resistances inherent to GAA devices (Chapter I). The standby current can be related to the very low n-channel threshold voltage before irradiation (V_{thn} = 0.2V). The nominal supply voltage V_{dd} is 3V. The operating frequency is 100kHz and can be increased up to 1MHz.

Table 6.2: Performance of the 1k GAA SRAM before irradiation.

Technology	3µm MESA isolated CMOS GAA
Cell type	6-transistor
Cell area	58µm × 111µm
Chip area	2.85mm × 4mm
Access time	< 150ns (@ 3V, 25° C)
Minimum Write Pulse	< 100ns (@ 3V, 25° C)
Standby current	< 2mA (@ 3V, 25° C)

The bias applied during irradiation is such that memories are in retention mode with all cells isolated (no read nor write operation). Input addresses are kept at the supply voltage to induce the worst degradations. No attempt was made to control the pattern during irradiation so that the imprinting effect of the preferred state can be easily observed. The irradiation has been stopped at different doses to check the global functionality of each memory with complementary checkerboard and diagonals patterns, using an HP16500B logic analysis system. One out of six memories was still fully functional after 85Mrad(Si) irradiation. The most critical part of the other memories is the lower half of the cell array for which the Word Line signal is regenerated by a CMOS buffer. The reason could be a wrong internal timing when the p-drive capability reduces.

The evolution of the threshold voltage shifts is similar to what has been presented in Figure 5.12 and is summarized in Table 6.3. V_{thn} rebounds approximately around 1Mrad(Si).

Table 6.3: Threshold voltage shifts of GAA devices as a function of dose and gate bias during irradiation.

	V_{thn}		V_{thp}	
Dose - V_G	0V	3V	0V	3V
pre-rad	0.35V	0.37V	-0.73V	-0.70V
1.6Mrad(Si)	0.32V	0.19V	-0.97V	-1.18V
85Mrad(Si)	0.65V	0.61V	-1.40V	-1.91V

The memory consumption is plotted in Figure 6.29 as a function of dose for two different patterns. The consumption measured in retention mode (static mode) starts from 1mA before irradiation, peaks at about 2mA around 1Mrad(Si), when the n-channel threshold voltage is minimum, and then steadily drops up to the highest dose due to the rebound of V_{thn}. The consumption measured when the memory is continuously read at 100kHz (dynamic mode) is only slightly larger than the static consumption (the dynamic consumption lower than the static consumption observed at very low dose for the "state-

1" diagonal pattern is not relevant). Hence, leakage currents dominate the transient currents necessary to charge (and discharge) the internal and output capacitances.

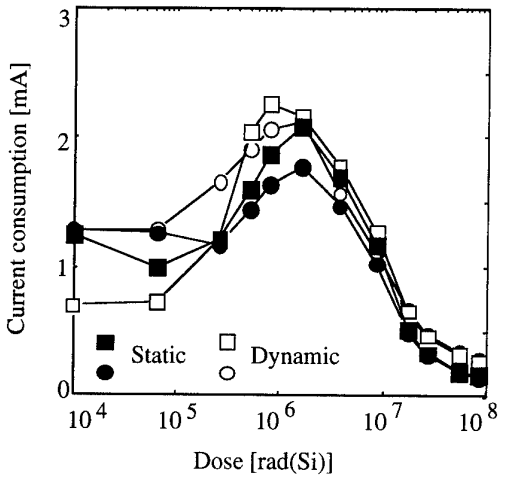

Figure 6.29: Static and dynamic memory consumption of a 1k GAA SRAM operated with checkerboard (circles) and "state-1" diagonal (square) patterns at 100kHz as a function of irradiation dose. V_{dd} = 3V.

A preferential state appears in the memory cell after only 100...250krad(Si) irradiation (imprinting effect due to the bias difference between the two cross-coupled inverters during irradiation) and is reinforced with increasing dose since no attempt was made to control the memory pattern during irradiation. This imprinting can be correlated to leakage currents. Indeed, the static leakage current is not the same when the cell is (minimum leakage) or is not (maximum leakage) in its preferential state. As a consequence, a variation of the global static consumption should be observed as a function of the pattern stored: the pattern which best matches the majority of the preferential states should have the lowest consumption. This effect can be easily observed when static leakage is maximum (around 1Mrad(Si)) as shown in Table 6.4. When the mean preferential state of the memory is less than 0.5 (more "state-0" than "state-1" preferred), the pattern imposing the largest amount of "state-0" ("state-1" diagonal) has the smallest consumption followed by the checkerboard pattern (equal number of "state-0" and "state-1") and the "state-0" diagonal. The global order is reversed when the mean preferential state is 0.62.

Table 6.4: Static consumption of a 1k GAA SRAM filled with different patterns after 1.6Mrad(Si) irradiation. V_{dd} = 3V.

Mean cell preferred state	Diagonal "state-1"	Checker-board	Diagonal "state-0"
0.26	1.1mA	1.8mA	2.4mA
0.36	1.4mA	1.6mA	1.8mA
0.62	2.1mA	1.8mA	1.4mA

The rise time τ_R and fall time τ_F were calculated between 10% and 90% of the rising or falling edges of the output signal and are depicted in Figure 6.30. The output load

capacitance is evaluated to be 15pF as mainly fixed by the input capacitance of the digital scope.

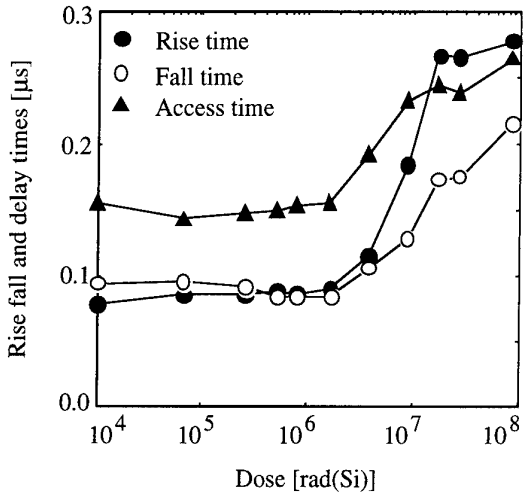

Figure 6.30: Rise, fall and access times of a 1k GAA SRAM as a function of irradiation dose. V_{dd} = 3V.

The rise time increases steadily since the p-channel transconductance drops under the combined effect of reduced mobility and reduced gate voltage overdrive (V_{dd}-V_G+V_{thp}). Since both ΔV_{thp} and $\Delta\mu_p$ are accentuated above 1Mrad(Si) due to delayed interface state generation (Chapter V), the increased of the rise time is also more pronounced above 1Mrad(Si). On the other hand, the fall time is stable or even decreases up to 1Mrad(Si) because, before the rebound of V_{thn}, the n-type gate voltage overdrive (V_G-V_{thn}) increases and compensates the mobility reduction. Again a severe increase of τ_F is observed above 1Mrad(Si) when interface traps are generated and imply a serious degradation of μ_n and the rebound of V_{thn}. After 85Mrad(Si), τ_R and τ_F are multiplied by a factor of about 3 and 2, respectively. The access time τ_A, measured between the points where the rising edges of the enable and output signals reach 50% of their final value, approximately follows the evolution of the fall time.

One can find in the literature a 64k SOI SRAM [18], a 64k SOS SRAM [11] and a 256k SOI SRAM, all from Harris, with a 1Mrad(Si) hardness. A 16k SOI SRAM from Honeywell [19] has been tested successfully up to 50Mrad(Si), and the higher irradiation level on complex circuits ever reported was performed on CMOS/SOI 16-bit microprocessors by the LETI in France [13] up to 100Mrad(SiO_2). At the light of these achievements obtained with state-of-the-art processes, the above results concerning the GAA technology up to 85Mrad(Si) with neither the design nor the process specially optimized for radiation hardness, demonstrate the intrinsic very good performance of the double-gate structure.

3.4. Conclusions

This chapter dealt with design assessment for SOI CMOS static memory circuits in total-dose environments. The main concern are large negative n-channel threshold voltage shifts, and hence leakage currents, created by charge trapping in the buried oxide. It has

been shown that peripheral circuits (such as simple inverters, logic gates embed in decoders, read differential amplifiers and output buffers) can resist large negative V_{thn} shifts if they are provided with adequate local compensation circuits. The "pull-up" configuration helps to keep a full logic swing, while the "diode-pair" configuration minimizes the shift of the inverter's switching point. Buffers including both "pull-up" and "diode-pair" stages combine both these advantages. However, those leakage-free designs stabilize the output characteristics upon radiation exposure at the expense of large area consumption and reduced speed. For these reasons, compensation circuits cannot be inserted in memory cells which are therefore the weakest elements of SRAMs. Numerically solving current equations and/or using HSpice simulations, the impact of layout parameters and threshold voltage shifts on the stability of a 6-transistor CMOS memory cell was evaluated in retention mode and during read and write operations. It arises that memory failure linked to leakage currents in n-channel devices cannot be overcome by proper design, except by using p-type accessed cells. The tremendous drawback of this solution is the drastic increase of the memory access time. The only practical solution hence consists in limiting the threshold voltage shifts to reasonable values by removing the buried oxide. The GAA technology being the perfect candidate, its potentiality has been evaluated by irradiating a 1k SRAM up to 85Mrad(Si). The GAA memory is still functional up to the highest dose but its access time has been multiplied by a factor of 3. The hardness of this memory when irradiated by heavy particles will now be examined.

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Chapter VII: Single-Event-Upset hardness of a 1k GAA SRAM

The first environment in which Single-Event-Effects (SEE) were experienced was space in 1975 [1]. Even today, space is the environment in which the vast majority of SEE has been recorded, but SEE have also been seen in other environments, such as in the atmosphere (during flights) [2,3], or in the vicinity of nuclear reactors, radioisotopic sources and accelerators [4]. The demand for SEE-resistant circuits is therefore very widespread. The advantages of SOI for producing Single-Event-Upset (SEU) hardened static random-access memories have long been known [5,6,7,8] because the buried oxide limits the collection length of charges created by heavy ions strikes. None of the charges generated in the substrate can be collected by the device junctions, except through a capacitive coupling across the buried oxide layer, if the top of the substrate is depleted. The thinner the SOI film, the better the SEU hardness. The SEU sensitivity of floating body SOI MOSFETs is however slightly increased due to the amplification of photocurrents by the parasitic bipolar transistor.

This chapter presents the SEU performance of a GAA static memory, the 1k SRAM described in Chapter VI actually. This circuit should exhibit the same strong SEU hardness than equivalent SOI circuits because the GAA silicon film is very thin and totally isolated as in SOI devices. Surprisingly, the SEU hardness of GAA SRAMs operated at 2V is better than the performance already reported for regular SOI memories operated at 5V. This result is very strange since lowering the supply voltage reduces the noise margin of the memory cell and hence should increase the SEU sensitivity.

The particular geometry of the GAA device which introduces important capacitances/resistances in the cross-coupling of the memory cell is mainly responsible for the excellent results. However, to obtain an accurate explanation of the strong SEU hardness, one should examine three points: the charge injected in the active film by the particle hit, the charge collected by the drain electrode which forms the current spike, and the charge necessary to flip the memory cell, also called critical charge. This study can be generalized to other SRAMs.

First, it will be shown that, when grazing ion beams are used, the injected charge in thin Si films is smaller than usually predicted. Secondly, simulations indicate that collection mechanisms and bipolar amplification are delayed in GAA devices. As a consequence, partial recovery of the cell state occurs, which means that the critical charge

for cell upset increases during the collection process. The determination of the cell upset conditions based on a purely static approach is hence no longer valid. The third point consists in the derivation of a general analytical model describing the time-dependence of the cell critical charge, independently of the current pulse shape generated by the ion. This model allows for a precise understanding of the influence of reduced supply voltage and naturally high Miller capacitances of the GAA memory cell. Finally, introducing time as a new variable, experimental data are explained.

1. Experimental data

The SRAMs described in Chapter VI were tested using the CYCLONE cyclotron of Louvain-la-Neuve, Belgium. Some details about the characteristics of the CYCLONE, the experimental procedure and the check for the validity of the results are presented in the Annex I. SRAMs were filled with a checkerboard pattern and continuously read under irradiation but no attempt was made to correct upsets when they occur. The cell states were frequently reversed in order to avoid an "imprinting" effect due to equivalent total-dose accumulation. The beam was composed of five different ions: N, Ne, Ar, Kr and Xe, in increasing order of LET_0, the Linear Energy Transfer of the normally incident particle. Selecting the ion with the highest LET_0, namely the 459MeV-xenon ion with $LET_0 = 55.9[MeV.cm^2/mg]$, tests were performed at different supply voltages ranging from 3V down to 1.9V. No upset was measured. We had to artificially increase the LET, by tilting the device under test by an angle of 60°, with the supply voltage reduced below 2.3V, to see some upsets within reasonable time intervals (3 hours).

Further tilting the device, the memory cross-section can be recorded as a function of the effective Linear Energy Transfer (LET_{eff}):

$$LET_{eff} = LET_0/\cos\theta$$

with θ the beam impinging angle. Tilt angles above 72° could not be used reliably due to a shadowing effect from the memory package. The resulting normal cross-section per bit $\sigma_0 = \sigma_m/\cos\theta$, with σ_m the measured cross-section [9], is represented by curve E in Figure 7.1 as a function of LET_{eff}. Curve E was recorded with $V_{dd} = 1.9V$, the minimum supply voltage still allowing correct memory operation. The asymptotic value of σ_0 should correspond to the physical area under the gate A_g, evaluated by:

$$A_g = M_N W_{eff}\left[L_{eff} - t_{si}tg(\theta)\right] = 1.9\times10^{-7}\left[cm^2/bit\right]$$

with $M_N W_{eff} = 4 \times 3\mu m$ the effective device width of the n-channel driver transistor of the SRAM cell (Figure 7.7), L_{eff} the effective device length and t_{si} the silicon film thickness. Figure 7.1 shows that the normal cross-section σ_0 is below $3\times10^{-8}[cm^2/bit]$ for LET_{eff} up to $170[MeV.cm^2/mg]$ and hence that the predicted asymptotic value is not reached up to the highest LET_{eff} investigated. The LET_{eff} threshold is around $100[MeV.cm^2/mg]$. To our knowledge, these devices present the highest SEU hardness ever obtained with such a low supply voltage. Figure 7.1 compares our result with bulk and SOI cross-sections obtained under a supply voltage of 5V: previously published results present a LET threshold below $50[MeV.cm^2/mg]$ [5,10,11].

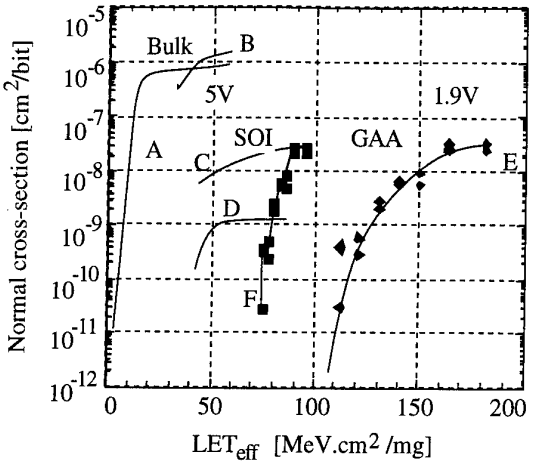

Figure 7.1: Normal cross-section per bit as a function of LET_{eff} given by (7-1) for bulk and SOI SRAMs: A: bulk (V_{dd} = 5V) [11], B: bulk (V_{dd} = 5V) [5], C: 500nm-thick SOI (V_{dd} = 5V) [5], D: 150nm-thick SOI (V_{dd} = 5V) [10], E: 85nm-thick GAA (V_{dd} = 1.9V), F: 85nm-thick GAA (V_{dd} = 1.9V) *vs.* LET_{eff} given by (7-3).

Figure 7.2 shows the evolution of the normal cross-section as a function of the supply voltage for $\theta = 70°$ corresponding to $LET_{eff} = 163[MeV.cm^2/mg]$. The sensitivity to V_{dd} is obvious: σ_0 falls from $3\times10^{-8}[cm^2/bit]$ at 1.9V down to only $5\times10^{-10}[cm^2/bit]$ at 2.3V. At the nominal supply voltage V_{dd} = 3V, we can only provide an upper bound because no upset has been recorded: the cross-section is far below $2\times10^{-11}[cm^2/bit]$. The total equivalent cumulated dose received by the components during this heavy ion test can be evaluated by [12]:

$$D[\text{rad(Si)}] = 1.6\times10^{-5}\cdot LET\left[MeVcm^2/mg\right]\cdot\phi\left[cm^{-2}\right]$$

with ϕ being the fluency. Considering all successive SEU measurements, the 1k SRAMs received about 1Mrad(Si) equivalent cumulated dose of irradiation. The effects of total-dose on SEU results will be discussed in the last section of this chapter.

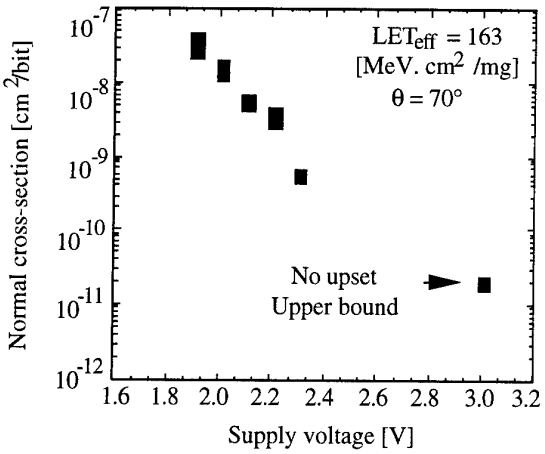

Figure 7.2: Normal cross-section per bit of a 1k GAA SRAM as a function of the supply voltage for $LET_{eff} = 163[MeV.cm^2/mg]$ (corresponding to a tilt angle of 70°).

In order to see some upsets with V_{dd} = 3V, the nominal supply voltage, memories were submitted to a high fluency beam (with a normal incidence). This experiment could not be performed with the xenon beam because too few xenon ions were accelerated. We used 150MeV-argon ions with LET_0 = 14.1[MeV.cm^2/mg]. The fluency was so high that particles could not be counted individually. The number of particles striking the device was deduced from the particle charge and the beam current: 500pA during 8 minutes. No upset was recorded. The cross-section was less than 5.24×10^{-14}[cm^2/bit]. The total equivalent cumulated dose was 4.3Mrad(Si) and confirms the excellent total-dose behavior of the GAA structure.

The excellent SEU performance of GAA devices has been obtained without introducing any design modification of the 6-transistor memory cell such as adding transistors/resistors [6] or Miller capacitors [7] in the cross-coupling to slow down the feedback, or using numerous additional transistors to restore data when corrupted by an ion hit [13]. The SEU hardness is therefore inherent to the GAA technology only. This strong hardness under low supply voltage will now be explained.

2. Injected charge

Basically, the strong SEU hardness experimentally observed in SOI/GAA circuits is obtained owing to the isolation of the active silicon device from charges injected into the substrate. Generally, the number of electron/hole pairs created is assumed to vary linearly with the length of the ion path. In SOI, the total amount of injected charges susceptible to be collected at one electrode, Q_{inj}, depends therefore on the silicon film thickness t_{si} and on the impinging angle θ:

$$Q_{inj} = LET_0 \bullet \frac{t_{si}}{\cos\theta} = LET_{eff} \bullet t_{si} \qquad (7\text{-}1)$$

with LET expressed in C/µm. Statistical variation of the energy deposition [14,15] will not be taken into account here while the presence of the top passivation SiO_2 layer [16] may be neglected within 10% precision. This is proved in Figure 7.3 and Table 7.1 showing the relationship between the tilt angle and the length of the ion path in the 1µm-thick top SiO_2 layer and in the 85nm-thick active Si film.

Table 7.1: Dependence of the xenon ion LET as a function of the path length (longitudinal dependence).

x [µm]	0	6.6	11.5	15.5	19	21.7	22.8	24	25.2	26.5	27.9	29.4	30.7
LET [pC/µm]	0.58	0.58	0.58	0.57	0.55	0.52	0.51	0.50	0.46	0.43	0.38	0.37	0.31

Up to $\theta = 85°$, the total path length before reaching the buried oxide does not exceed 15µm. Since the xenon ion LET is nearly constant within the first 20µm of its trajectory, the influence of the top SiO_2 layer can be neglected and the injected charge follows, up to now, relationship (7-1). However, geometrical factors [15,16] related to the smallest dimension of the active volume are known to introduce a discrepancy between the

formulation (7-1) and the energy really deposited. We will show that such a spatial reduction exists in thin and ultra-thin SOI/GAA devices for grazing ion beams due to the radial extend of the track.

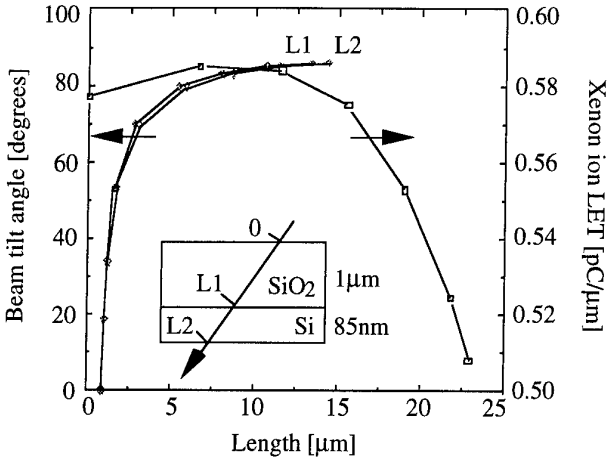

Figure 7.3: Xenon ion LET and beam tilt angle as a function of the path length in the 1µm-thick SiO_2 passivation layer (L1) and in the 85nm-thick Si film (L2).

Let us use the classical assumption that the radial distribution R(r) of the electron/hole plasma is a gaussian function with a characteristic radius (1/e distance) R_c equal to 0.1...0.2µm [17,18]. In thin and ultra-thin SOI devices, R_c is comparable to or even larger than half the silicon film thickness. Therefore, when the ion impinging angle increases, only a fraction X of the total charge (7-1) is effectively generated within the silicon active area. As a result, LET_{eff} is reduced. For a horizontal track through drain, channel and source ($\theta = 90°$), centered in the middle of the film, this fraction X is very easy to compute analytically. X[θ=90°] is indeed simply the integral of the gaussian distribution from the bottom interface to the top surface of the film:

$$X[\theta=90°] = 2\int_0^{t_{si}/2} R(r)dr = \mathrm{erf}\left(\frac{t_{si}/2}{R_c}\right) \qquad (7\text{-}2)$$

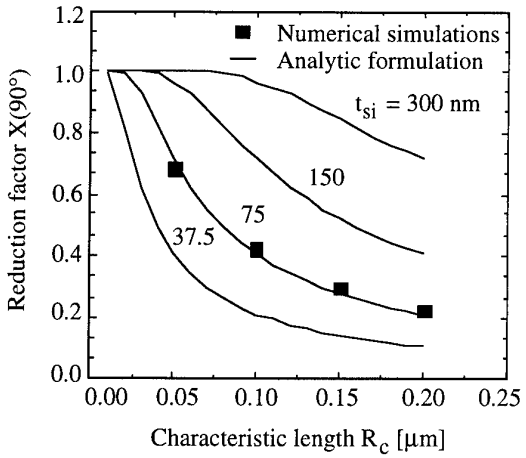

Figure 7.4: Reduction factor X[θ=90°] of the injected charge as a function of the characteristic radius R_c of the gaussian radial distribution of the track with t_{si} as parameter. Horizontal strike from drain to source.

Figure 7.4 plots this fraction X[θ=90°] as a function of R_c with t_{si} as parameter. It is clear that two-dimensional Medici simulations (dots) correctly follow the analytic formulation. t_{si} is increased by a factor of 2 from one curve to another. X[θ=90°] could be as small as 0.24 for t_{si} = 85nm and R_c = 0.2μm. Since θ is maximum in (7-2), this relationship only provides the lower boundary of the reduction factor. The evolution of X as a function of the tilt angle is shown in Figure 7.5 for t_{si} = 85nm with R_c as parameter. Although X[θ] is close to unity for small impinging angles, it must be accounted for, in thin SOI, as soon as θ > 30° and it decreases nearly linearly for θ > 40°. Since the incident angles involved in our experiment varied between 60° and 73°, X[θ] was comprised somewhere between 0.8 and 0.5 considering 0.1μm < R_c < 0.2μm. This advantageous geometrical charge injection reduction for grazing ion beams is here analyzed as a function of R_c but can also be expressed as a function of the cut-off energy of secondary electrons and the chord length of the active volume [15].

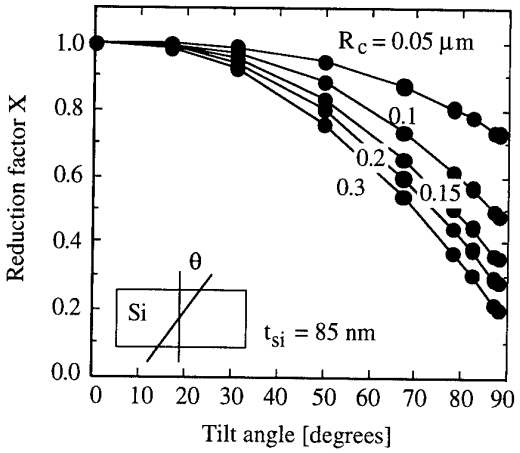

Figure 7.5: Geometrical reduction factor X of the injected charge as a function of the tilt angle θ with R_c as parameter. t_{si} = 85nm.

Taking X into account, the injected charge is then finally given by:

$$Q_{inj} = LET_0 \bullet \max\left\{\frac{t_{si}}{\cos\theta}, L\right\} \bullet X[\theta] = LET_{eff} t_{si} \qquad (7\text{-}3)$$

When the experimental cross-section is plotted as a function of the corrected value $LET_{eff} = LET_0 X[\theta]/\cos\theta$ for R_c = 0.2μm, curve E moves to curve F in Figure 7.1 and defines a smaller and sharper LET_0 threshold around 70[MeV.cm²/mg] for normally incident ions, value which is closer to (but still better than) previously published results.

3. Collected charge

Although the charge injected in the sensitive part of SOI devices is efficiently limited by the buried oxide layer, especially for large impinging angles, its effect is susceptible to be strongly enhanced by the parasitic bipolar action of the floating body [19]. Indeed, in a SOI/GAA nMOSFET without body tie, holes created by the heavy particle cannot escape through the substrate electrode. They travel to the source, accumulate there, raising the body-to-source potential which, in turn, results in an increase of the electron current to

the drain. As a consequence, the charge collected by the sensitive electrode can be larger than the charge injected by the particle.

3.1. Simulation set-up

The bipolar action is so complex that it must be investigated by numerical simulations. Two-dimensional Medici simulations of xenon ion hits through SOI/GAA devices at different incident angles have hence been performed. The rectangular mesh reproduced the structure resulting from the GAA process with a 85nm-thick silicon film and front/back gate oxides of 30nm (Figure 7.6). The effective channel length L_{eff} was 2.4µm.

The model used by Medici included Schockley-Read-Hall recombination with concentration dependent lifetime, Auger recombination, carrier-carrier scattering which includes the dependence of mobility on doping and temperature, and field-dependent mobility. To simplify the problem and because we work with long devices and reduced supply voltage, the local electric field-dependent impact ionization model was turned off. The default value of carrier lifetimes (0.1µs) was adopted because it constitutes a reasonable estimation for the SIMOX technology. The generation term G in the continuity equations is described by G = T(t) R(r) L(x) where x is the distance along the ion track, r is the radial distance to the ion trajectory and t is time. The chosen function for T(t) is gaussian with a characteristic time equal to 1.5ps. R(r) is also gaussian with a chosen characteristic radius R_c = 0.2µm, and L(x) is described in Table 7.1. Although Medici adopts a 1µm-wide slice of silicon where the generation is considered as uniform in the third dimension, qualitative trends can be highlighted from these two-dimensional simulations.

We focus on the situation where the energetic ion strikes a n-channel transistor in the off-state, called n-hit (strike at node V_1 in Figure 7.7), since it is well known that n-hits require less charge to cause cell upset than p-hits [20]. Only the n-channel struck device was simulated in Medici with its drain loaded by a resistance R_T and a capacitance C_T in parallel, replacing all other transistors of the cell. Gate and source terminals were grounded. The equivalent capacitance C_T depends on the different parasitic capacitances of the GAA transistor, represented in Figure 7.6, and listed in the Annex II for a minimal size square transistor.

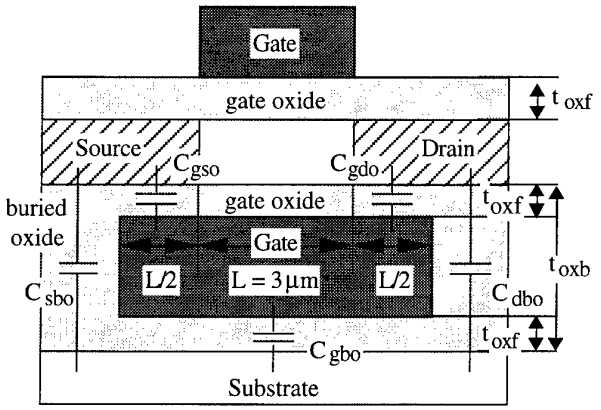

Figure 7.6: Longitudinal cross-section of GAA devices and location of the different parasitic capacitances.

The main differences, when compared to classical SOI devices, are the relatively high gate-to-substrate capacitance C_{gbo} across an oxide as thin as the gate oxide and the important overlap gate-to-source/drain capacitances $C_{gd,so}$ due to the extension of the back portion of the gate 1.5μm below the source and drain regions. At the cell level, those different parasitic capacitances, together with the gate capacitances, can be grouped in three terms as shown in Figure 7.7: C_1 (C_2) between the hit node V_1 (the other internal node V_2) and ground, and C_3 the non-negligible cross-coupling capacitance. The detailed derivation is provided in the Annex II and yields: $C_1 = 80$[fF], $C_2 = 86$[fF], $C_3 = 84$[fF]. Assuming a perfect capacitive coupling between V_2 and V_1, the total capacitance seen by the hit node is:

$$C_T = C_1+C_2C_3/(C_2+C_3) = 0.12 \text{ [pF]} \quad (7\text{-}4)$$

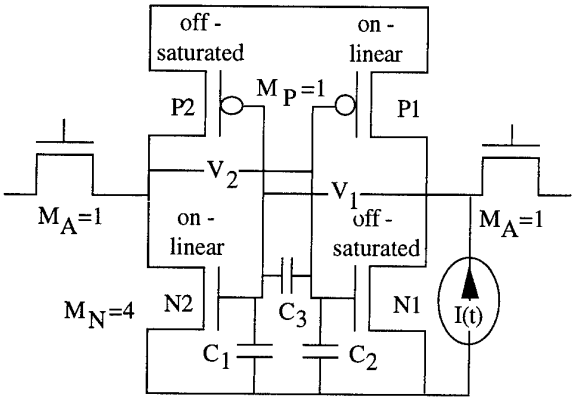

Figure 7.7: The SRAM memory cell design.

The equivalent resistance R_T increases with reduced supply voltage as presented in Table 7.2 where n- and p-threshold voltages are equal to 0.2V and -0.7V, respectively. R_T mainly represents the driving capability of the on-biased p-type pull-up device P1 of the memory cell (Figure 7.7). R_T was extracted by fitting from Spice simulations. The fitting consists in obtaining the same variation of the drain potential (if no switching occurs) when the struck transistor is inserted in the full cell or is loaded by C_T and R_T in parallel. This fitting is nevertheless unnecessary and a rough estimation of R_T is sufficient because, as it will be shown, Medici simulations are insensitive to this parameter. Also, a reasonable estimation of R_T will be provided later on in (7-8).

Table 7.2: Equivalent resistance of the GAA memory cell as a function of the supply voltage.

V_{dd} [V]	3.5	3	2.6	2.4	2.2	2	1.9	1.8	1.7	1.6	1.5
R_T [kΩ]	13	15	17	21	25	35	40	45	55	65	80

Although R_T and C_T correctly represent the mean loading behavior of the cell at the drain of the struck device, simulations cannot determine if the particle strike ultimately will result in a cell upset, since the device is not inserted in a flip-flop configuration. A very recent publication [21] points out the dramatic effects of external circuit loading on

the charge-collection response of a hit transistor and recommends to use a three-dimensional mixed-mode simulation tool. In this case, the struck device is simulated at the device level while the other transistors of the cell are simulated at the circuit level. We could not performed such simulations since the mixed-mode module of Medici was not yet available in our laboratory. The purpose of the next section is therefore to sketch the general evolution of the collected charge as a function of various parameters. Results should be correct before the switching time, at least qualitatively. On the other hand, three-dimensional simulations will be presented in the last section of this chapter, when the precise comparison of critical and collected charges are necessary to deduce the upset conditions.

3.2. Physical mechanisms

Figure 7.8 depicts, for a supply voltage of 2V, the time dependence of the drain potential pulse V_D and the drain current spike I_D which appear when a xenon ion crosses the GAA device horizontally from drain to source in the middle of the film. The collected charge at time t, also shown in Figure 7.8, is the integral of the drain current up to time t:

$$Q_{col}(t) = \int_0^t I_D(t)dt .$$

Three different physical mechanisms can be successively distinguished:

- charge injection from 10^{-13}s to 10^{-11}s
- direct ion shunt effect [22] from 10^{-11}s to 10^{-9}...10^{-8}s
- parasitic bipolar amplification [5,19,22] from 10^{-9}...10^{-8}s to 10^{-6}s.

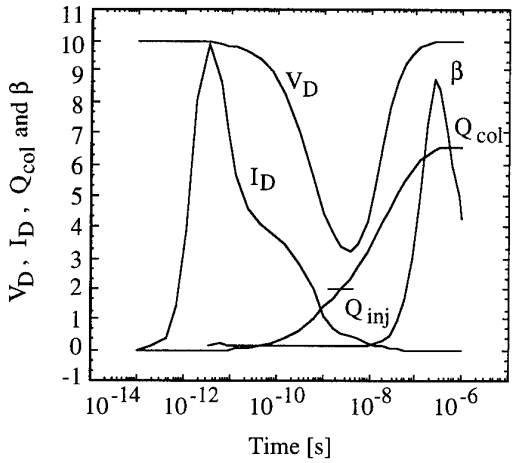

Figure 7.8: Time evolution of
a) the drain voltage $V_D \times 0.2V$
b) the drain current $I_D \times 10^{-4}A$
c) the normalized collected charge $Q_{col}/Q_{inj} \times 0.5$
d) the bipolar gain $\beta \times 10$
for a horizontal xenon ion strike from drain to source in the middle of the film, with $V_{dd} = 2V$.

- The direct ion shunt

The carrier injection, nearly uniform in the whole device for horizontal tracks, is so high, that the electron concentration in the body reaches the source and drain doping

levels (10^{19} cm^{-3} in the body and 2×10^{19} cm^{-3} in source/drain regions). Therefore, the ion track acts as a plasma directly shorting the source and drain regions of the same type. Although the carrier concentration is not rigorously uniform so that the non-equilibrium ambipolar diffusion should play some part, the transistor can be viewed as a purely resistive silicon bar. This is clearly visible in Figure 7.9, which depicts the body potential at logarithmic time intervals: around $10^{-11}...10^{-10}$s, the potential is nearly linear between the source and drain contacts. The electric field E is therefore approximately constant throughout the structure and is roughly given by:

$$E(t) = \frac{V_D(t)}{Ls + Ld + L} = \frac{V_{dd} - Q_{col}(t)/C_T}{Ls + Ld + L} \tag{7-5}$$

with L the gate length, Ls and Ld the lengths of source and drain diffusions respectively. As a consequence, important drift (and probably diffusion) currents of electrons and holes flow in the device (Figure 7.8). This prompt charge collection mechanism, which can be associated to the funnel effect occurring in the substrate of bulk devices, collects charges slowly compared to the bulk case and even to the regular SOI case. Indeed, the electric field, which controls the drift current, is especially weak in the GAA structure owing to both low supply voltage (1.9V) and large values of Ls (5µm) and Ld (5µm) in relationship (7-5).

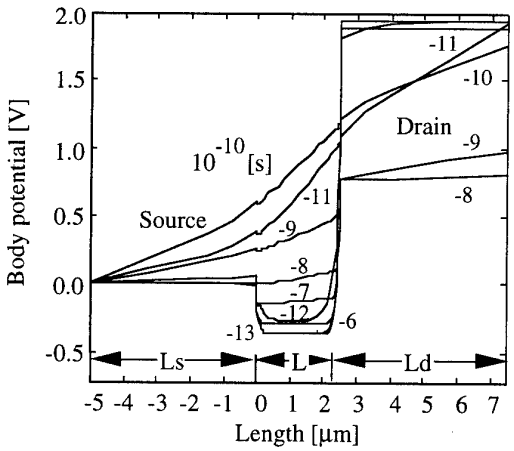

Figure 7.9: Evolution with time of the body potential for a horizontal xenon ion strike with V_{dd} = 2V.

• The bipolar amplification

After about 1ns, Figure 7.9 shows that the reversed-biased potential barrier at the drain junction starts to rebuild and that the electric field in the channel region collapses such that the direct shunt stops [22]. The hole current, collected at the source where the junction is forward-biased, is now small compared to the electron current so that the carrier transport resembles that typical of a bipolar transistor [5,19,22]. The current gain is defined by the ratio $\beta = J_{ns}/J_{ps}$ where J_{ns} and J_{ps} are the instantaneous current densities of electrons and holes at the source respectively. β, also added in Figure 7.8, starts from a low value characteristic of high injection conditions, increases after 10ns as the carriers in excess are evacuated and tends towards a maximum value related to the emitter efficiency. The maximum theoretical value of β, related to the source and channel doping concentrations, is approximately equal to 75. This parasitic bipolar mechanism is responsible for a non-

negligible amplification of the injected charge. The multiplication factor is defined as the collected charge normalized to the injected charge, $\beta_{eff}(t) = Q_{col}(t)/Q_{inj}$ [23] with Q_{inj} given by (7-3). β_{eff} can be evaluated by comparing Q_{col} and Q_{inj} in Figure 7.8. β_{eff} is around 1.6 after 10^{-8}s and 3.3 after 10^{-6}s. Fortunately, the enhancement of the collected charge occurs very late.

The physical mechanisms inducing charge multiplication are now clearly identified and allow one to investigate the modifications of the collected charge as a function of various parameters.

Figure 7.10 shows $Q_{col}(t)$ with the impinging angle as parameter. Q_{col} is sensitive to θ in the direct shunt phase as well as in the bipolar amplification region. Hits are located through the middle of the gate as indicated in the inset of the Figure. With $\theta < 80°$ and $L_{eff} = 2.4\mu m$, the ion track no longer directly connects the source and drain regions and the prompt collection related to the ion shunt mechanism virtually disappears. Nevertheless, even for small θ, when the hit occurs near the drain region (dotted curve for $\theta = 80°$), some kind of funneling effect extends the depletion region controlled by the drain and sucks up the electrons such that Q_{col} increases earlier. Therefore, not only the incident angle but also the location of the ion strike is of importance. Horizontal dotted lines indicate the injection level Q_{inj} for the different incident angles and help to observe that the amplification factor β_{eff} strongly increases when the injection level (and hence θ) decreases. For example, $\beta_{eff}(67°)/\beta_{eff}(90°)$ is equal to 3.2/1.7 = 1.9 at 10^{-8}s and to 10.45/3.36 = 3.1 after 10^{-6}s.

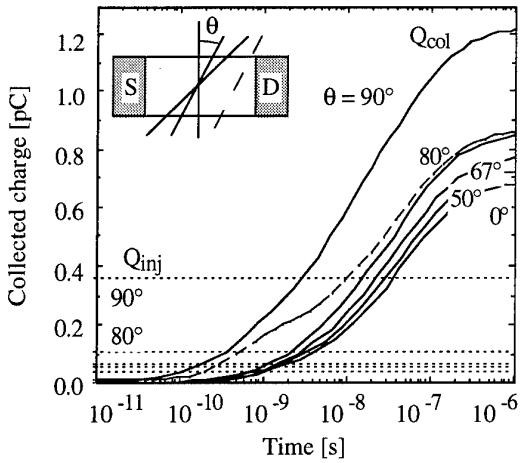

Figure 7.10: Evolution with time of the collected charge as a function of the tilt angle and the position of the hit. V_{dd} = 2V. Plain lines: hits through the middle of the gate. Dashed line: hit close to the drain. Horizontal lines: injection level Q_{inj} increasing with the tilt angle.

In Figure 7.11, modifications of Q_{col} with other parameters are highlighted. Curves labeled * and ** are reference plots for $\theta = 90°$ and 67°, respectively. Other curves are obtained by changing only one parameter at a time. First, we focus on $\theta = 90°$ to investigate the direct ion shunt phenomenon. From the formulation (7-5) of the electric field, the key parameters influencing the ion shunt should be V_{dd}, C_T and L. Because Ls+Ld is huge in GAA transistors (10μm, related to the cavity overetching), no clear dependence on L is visible in Figure 7.11.

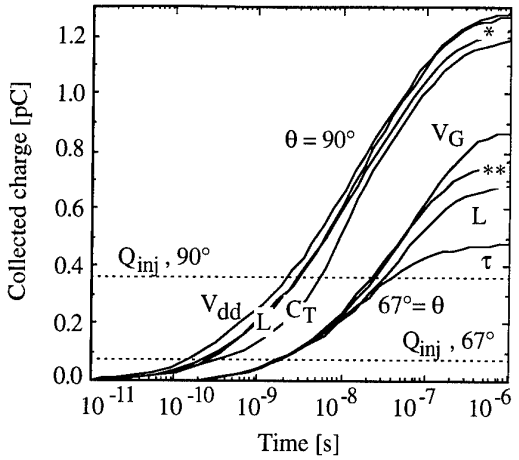

Figure 7.11: Sensitivity of the collected charge to various parameters:
*: reference curve for $\theta = 90°$ **: reference curve for $\theta = 67°$
obtained with $V_{dd} = 2V$, $L = 2.3\mu m$, $C_T = 0.17pF$, $\tau = 100ns$ and $V_G = 0V$.
The other curves are obtained when one parameter is changed at a time:

V_{dd}:	$V_{dd} = 3V$;	τ:	$\tau = 50ns$;
L:	$L = 3\mu m$;	V_G:	$V_G = 0.2V$;
C_T:	$C_T = 0.05pF$.		

The influence of V_{dd} is weak but nevertheless shows that an increase of the supply voltage (from 2 to 3V) enhances the charge collection by increasing the electric field. Finally, a reduction of C_T (from 0.17 to 0.05pF) not only reduces the drain voltage $V_D = V_{dd}-Q_{col}/C_T$ but mostly makes its drop earlier so that the electric field is reduced from the very beginning of the ion shunt mechanism. As a consequence, the charge collection is delayed. Here, the GAA structure, with its larger C_T value, is penalized compared to regular SOI devices.

The variations of the bipolar amplification factor β_{eff} are illustrated by the curves obtained with $\theta = 67°$. The amplification under high injection conditions ($...10^{-9}s... < t < ...10^{-8}s...$) is nearly insensitive to all parameters. As expected, for $t > ...10^{-8}s...$, β_{eff} decreases with shorter carrier lifetime (decreased from 100 to 50ns) or longer gate (extended from 2.3 to 3μm) at the condition that the hit is located at a constant distance from the drain junction. A surprising influence is that of the gate voltage which enhances the bipolar action when raised up to the threshold voltage. For $V_G > V_{thn}$, β_{eff} decreases again. The supply voltage could also have an indirect influence on β_{eff} because a reduction of the impact ionization (when V_{dd} is lowered) enhances the bipolar current gain [24]. Since the collected charge is computed with a reduced precision when a steady current flows through the device, the influence of the impact ionization and the gate voltage should be carefully verified.

Finally, we have observed that simulations are insensitive to R_T, the equivalent resistance of the memory cell. The explanation could be the following: R_T determines the recovery of the drain voltage, which occurs late, during the bipolar phase (Figure 7.8). The early ion shunt region is therefore obviously independent on R_T. The independence of the bipolar phase on R_T, on the other hand, is due to the insensitivity of β to the drain voltage (β being mainly determined by the source junction). Contrarily to R_T, we have shown that the capacitive load C_T is of huge importance. It should be noted that mixed-

mode simulations also lead to the conclusion that replacing the cell by a purely resistive load is not suitable for charge collection simulations [21], but, to our knowledge, no investigation of the capacitance loading influence has been published.

In summary, the collection of charges in GAA devices is slow because the early ion shunt effect is limited by the low supply voltage and source/drain series resistances, while the bipolar amplification is delayed due to high injection conditions. The collected charge has been shown to be a strong function of various parameters such as the supply voltage, the device length, the equivalent capacitance of the cell, the carrier lifetime and the gate voltage. Those parameters should be carefully fitted to experimental conditions to obtain simulations which could quantitatively explain measurements.

4. Critical charge

The determination of the cell upset conditions is based on the comparison of the collected charge Q_{col} and the critical charge Q_{crit} necessary to induce a change of the memory cell state. We have discussed Q_{col}, now we focus on Q_{crit}. Usually, a purely static approach is used where the total collected charge at a critical junction after an infinite time is compared to the critical charge Q_{crit}, supposed to be constant during the collection process. Q_{crit} is given by the time-invariant product of the total nodal capacitance C_T and the supply voltage [23,25]:

$$Q_{crit} = \alpha V_{dd} C_T \qquad (7\text{-}6)$$

C_T is given by (7-4) and α is a fitting parameter depending only on the technology. This static approach works well as long as the charge collection is prompt compared to the feedback reaction time of the memory cell. However, we have seen that the collection mechanisms are delayed in GAA devices. Therefore partial recovery of the cell initial state occurs owing to the current flowing through the pull-up pMOS transistor P1 of the memory cell (Figure 7.7). This partial recovery results in an increase of the critical charge during charge collection.

While still keeping the critical charge constant, some authors recently overcame this problem by adapting the definition of β_{eff} [23]. In Reference [26], the cell SEU sensitivity (Q_{crit}) is described by a characteristic deposition time which is unfortunately not clearly defined and is determined by means of numerous Spice simulations with different ion current pulse shapes. Finally, recent publications [21] stress the importance of including recovery and time in calculations of a critical charge to upset, but do not present any analytical formulation. In this section, we propose a new general time-dependent analytical model of the critical charge, neither dependent on the device physics (β_{eff}) nor on the ion current pulse shape.

Introducing time as a new variable, the following definition of the upset point arises: the cell upsets at time τ after the beginning of the ion hit if $Q_{col}(\tau)$, the total charge deposited on the capacitance at time τ, exceeds (for the first time) $Q_{crit}(\tau)$, the critical charge evaluated at that time. The basic assumption of the model is that the response of the struck node is independent of the system history. Therefore, the ion current pulse,

independently of its shape, is equivalent at time τ to a rectangular current pulse (of duration τ) providing exactly the same integrated charge at that time. The time dependence of the cell critical charge is hence fully determined by using rectangular pulses of increasing widths. For each pulse duration τ (applied to node V_1 of Figure 7.7), a minimum constant current $I_{crit}(\tau)$ is required to change the cell state, corresponding to a single minimum critical charge $Q_{crit}(\tau) = \tau.I_{crit}(\tau)$. As previously announced, this approach eliminates the problem encountered by several authors who try to replace the real current pulse by exponential functions and unfortunately observe a dependence of the critical charge on the chosen current shape. $I_{crit}(\tau)$ and $Q_{crit}(\tau)$, obtained by means of Spice simulations, are sketched in the log-log plot of Figure 7.12 (left and right part, respectively) for a classical GAA memory cell.

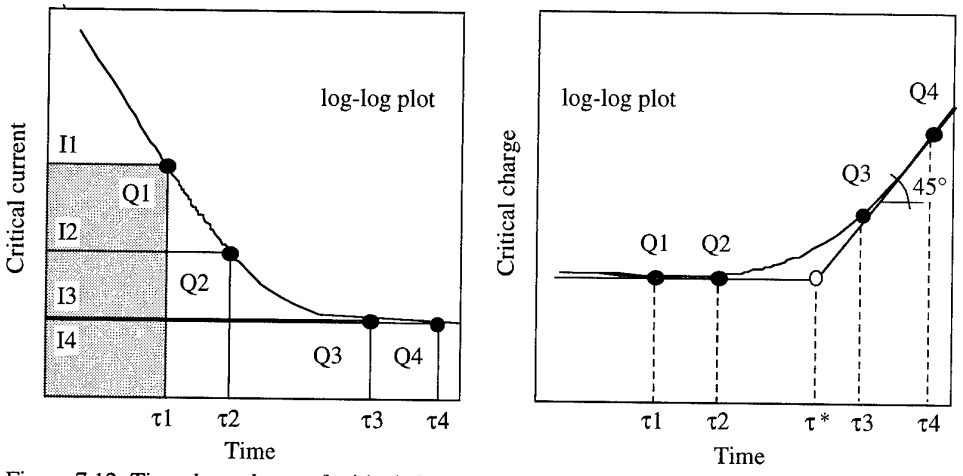

Figure 7.12: Time dependence of critical charge and critical current for GAA memory cell upset.

Figure 7.12 shows that, for a short pulse width ($\tau 1$, $\tau 2$), the minimum current necessary to upset the cell is inversely proportional to the pulse width and decreases steadily (I1, I2). Therefore, Q_{crit} nearly takes the usual constant value given by (7-6) (Q1, Q2). On the contrary, for longer pulses ($\tau 3$, $\tau 4$), the minimum current tends towards a constant value (I3, I4) that corresponds to the saturation current of the pull-up pMOS device P1 of Figure 7.7: $I_{P1,sat} = \mu_p C_{ox}(W/L)_p(V_{dd}-|V_{thp}|)^2/2$. As a consequence, Q_{crit} increases (Q3, Q4) and finally follows the pulse width linearly (which is indicated by a slope at 45° in the log-log plot of Figure 7.12).

Running numerical simulations for each constant current pulse width, in order to find $I(\tau)$ and $Q_{crit}(\tau)$, is very time consuming. Therefore, we will develop analytical models for $Q_{crit}(\tau)$.

4.1. First order model

A first very simple model giving the temporal evolution of Q_{crit} is the following:

$$\begin{aligned} Q_{crit}(\tau) &= \alpha V_{dd} C_T \\ Q_{crit}(\tau) &= I_{P1,sat}\tau \end{aligned} \quad \text{for} \quad \begin{aligned} \tau &\le \tau^* \\ \tau &> \tau^* \end{aligned} \qquad (7\text{-}7)$$

It assumes, that Q_{crit} is constant before the breaking point τ^* and is proportional to $I_{P1,sat}$ when time exceeds τ^*. The breaking point of the model τ^*, shown in the right part of Figure 7.12, corresponds to the feedback reaction time of the memory cell, since it determines the time at which recovery begins to appear and hence P1 to play a part. τ^* provides a clear definition of the cell equivalent resistance R_T since:

$$\tau^* = \frac{\alpha V_{dd}}{I_{P1,sat}} C_T = R_T C_T \tag{7-8}$$

This first model only contains one fitting parameter α. The best fitting between Spice simulations and relationship (7-7) is obtained, for the GAA technology, with $\alpha = 1.81$. Although simple, the model already enables us to understand the dependence of Q_{crit} on the capacitance C_T and the supply voltage V_{dd} as shown in Figure 7.13.

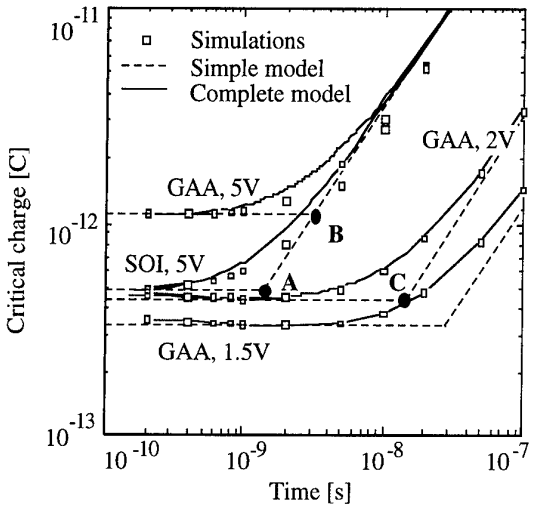

Figure 7.13: Time dependence of the critical charge as a function of the supply voltage (1.5V, 2V and 5V) and the capacitance (GAA: with $C_{gs,do}$ and C_{gbo}, SOI: without $C_{gs,do}$ and C_{gbo}).

• If the capacitance is increased with the same supply voltage $V_{dd} = 5V$, which is the case when GAA devices are used instead of regular SOI transistors, the breaking point moves from A to B in Figure 7.13: the plateau of Q_{crit} but also τ^* rise linearly with C_T in (7-7) and (7-8), respectively. Since $I_{P1,sat}$ is unchanged (which fixes the vertical position of the oblique line at 45°), Q_{crit} is only modified for short time after the ion strike.

• When V_{dd} is reduced from 5V to 2V with the same capacitance (C_T corresponding to GAA devices), the breaking point moves from B to C: the plateau of Q_{crit} decreases linearly with V_{dd} while τ^* increases following approximately V_{dd}^{-1} due to the reduction of $I_{P1,sat}$ in (7-8). As a result, the cell is upset sensitive for a much longer time.

• The comparison of points A and C indicates that, owing to the larger capacitance provided by the GAA technology, the supply voltage can be lowered while still maintaining the same minimum Q_{crit} value than in SOI devices. To quantify this improvement, C_T is computed with and without the parasitic capacitances $C_{gs,do}$ and C_{gbo} specific to the GAA process. A ratio 2.4 between the two expressions is obtained. However, this is not sufficient to conclude that the GAA supply voltage could be lowered 2.4 times below the SOI supply voltage while still presenting the same SEU hardness. Indeed, even if the minimum Q_{crit} value is the same, the breaking point of the model

moves to the right when the supply voltage decreases so that the GAA cell is sensitive to charge collection for a longer time than the SOI cell.

Although this first model roughly provides the correct trends as a function of variables C_T and V_{dd}, it clearly underestimates the critical charge by about a factor 2 at the breaking point τ^*, precisely in the most critical region for cell upset, as will be shown later on. A more refined model follows.

4.2. Improved model

First, we modify the equivalent capacitance of the memory cell. Since the hit n-channel device is in the off-state, V_1 is high and V_2 is low before the ion strike as shown in Figure 7.14. The strong coupling C_3 between internal nodes V_1 and V_2 of the memory cell implies that, when V_1 drops due to the ion hit, V_2 is also submitted to a negative shift and cannot be assumed to stay at the ground voltage as done previously [20]. On the other hand, the perfect capacitive coupling between V_1 and V_2 adopted in the simple model to define C_T in (7-4) becomes wrong when long switching times are involved, because it omits to take account for the recovery action of the inverter P2-N2. Therefore, the relationship between ΔV_2 and ΔV_1 is situated somewhere between purely static situation $\Delta V_2 = 0$ and perfect capacitive coupling $\Delta V_2 = C_3 \Delta V_1 / (C_3 + C_2)$. Hence, $\Delta V_2(t) = H.\Delta V_1(t)$ with $0 < H < C_3/(C_2+C_3)$. H will be defined in (7-12). The total capacitance at node V_1 becomes:

$$C_T^* = C_1 + (1 - H)C_3 \tag{7-9}$$

Then, the main idea is to consider, for long switching times, the recovery action of the current delivered by transistor P1 in Figure 7.7. In order to simplify the problem, the gate of P1 is supposed to be grounded (uncoupled to V_2). Therefore, as long as $V_1(t) > |V_{thp}|$, P1 works in the linear regime. Below $|V_{thp}|$ and down to the switching point, P1 is saturated (Figure 7.14). The switching time τ is such that $V_1(\tau) = V_2(\tau)$.

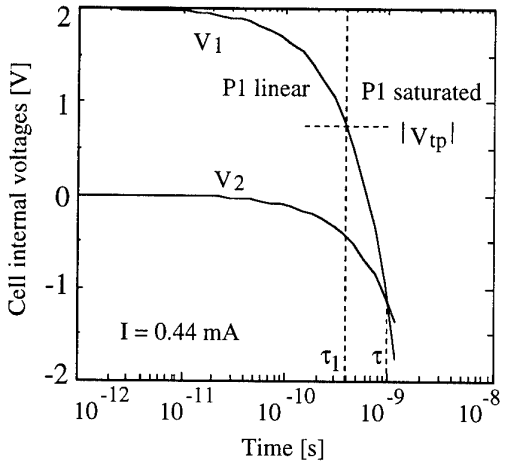

Figure 7.14: Evolution of the cell internal voltages (V_1 and V_2) as a function of time when a rectangular current pulse of 0.44mA is applied to node V_1.

• We compute time τ_1 such that P1 enters the saturation regime, $V_1(\tau_1) = |V_{thp}|$. Up to τ_1, the system is described by the following differential equation:

$$\frac{\partial V_1(t)}{\partial t} = \frac{I_{P1}(t) - I}{C_T^*}$$

with I the ion current and I_{P1} the current flowing through transistor P1:

$$I_{P1}(t) = \beta_p \left[\left(V_{dd} - |V_{thp}| \right) - \frac{\left(V_{dd} - V_1(t) \right)}{2} \right] \left(V_{dd} - V_1(t) \right)$$

where $\beta_p = \mu_p C_{ox} (W/L)_p$, as usual. The solution to this equation is:

$$V_1(t) = |V_{thp}| - b \bullet tg\left(\frac{b\beta_p}{2C_T^*} t - \delta \right)$$

with $b = \sqrt{2I/\beta_p - \left(V_{dd} - |V_{thp}| \right)^2}$ and $\delta = \text{arctg}\left(\left(V_{dd} - |V_{thp}| \right) / b \right)$.

The computation of τ_1 is straightforward and gives:

$$\tau_1 = \frac{2C_T^* \delta}{b\beta_p} \tag{7-10}$$

• Beyond τ_1, P1 delivers the constant current $I_{P1,sat}$ so that V_1 and V_2 depend now linearly on time (in Figure 7.14, the time is on logarithmic scale) and are described by:

$$V_1(t) = |V_{thp}| - \frac{I - I_{P1,sat}}{C_T^*} [t - \tau_1]$$

$$V_2(t) = -H\left(V_{dd} - |V_{thp}| \right) - \frac{H\left(I - I_{P1,sat} \right)}{C_T^*} [t - \tau_1]$$

The switching time τ, such that $V_1(\tau) = V_2(\tau)$, is:

$$\tau = \frac{\left[HV_{dd} + (1-H)|V_{thp}| \right] C_T^*}{(1-H)\left(I - I_{P1,sat} \right)} + \tau_1 \tag{7-11}$$

Recalling that the current delivered by the rectangular pulse I is constant, the critical charge is simply obtained by:

$$Q_{crit}(I) = I.\tau(I)$$

and corresponds to the plain lines of Figure 7.13. The implicit parameter I is provided by the slope of the vector joining $Q_{crit}(\tau)$ at the origin of the axes. Good agreement between this model and Spice-simulations (represented by dots in Figure 7.13) is achieved with the following variation of H as a function of I:

$$H(I) = \frac{C_3}{(C_2 + C_3)}\left(\frac{I - I_{P1,sat}}{I}\right)^h \qquad h = 0.5 \qquad (7\text{-}12)$$

Relationship (7-12) can be easily justified. When $\tau << \tau^*$ and $I >> I_{P1,sat}$ ($\tau 1$, I1 in Figure 7.12), H tends to $C_3/(C_2+C_3)$ as in the simple model. V_2 is only governed by capacitive coupling to V_1 and strongly decreases with time. On the other hand, for $\tau >> \tau^*$, I tends to $I_{P1,sat}$ ($\tau 4$, I4 in Figure 7.12). H decreases and takes account for the static action of the inverter N2-P2 that opposes to the capacitive coupling. The decreasing rate of H is fixed by the fitting parameter h. With h = 0.5, the global model, obtained by combining relationships (7-9) to (7-12), is very accurate for a wide range of capacitance and supply voltage variations as shown in Figure 7.13. However, the model slightly overestimates the critical charge for large supply voltages (V_{dd} = 5V) probably due to the hypothesis of grounded gate for P1.

It is possible to show that, when $I >> I_{P1,sat}$ ($\tau << \tau^*$), the critical charge tends to the constant value:

$$\lim_{\tau \to 0} Q_{crit}(\tau) = \frac{V_{dd} C_T^*}{1 - H} = \left[\frac{C_2 + C_3}{C_2}\right] V_{dd} C_T = \left[C_1 + C_3\left(1 + \frac{C_1}{C_2}\right)\right] V_{dd} \qquad (7\text{-}13)$$

Identifying (7-13) with (7-7), we find a physical interpretation for the fitting parameter α of the first model: α should be equal to the capacitive ratio $(C_2+C_3)/C_2$ = 1.97. This is verified since the best fitting value for α is 1.8. Finally, the last hand of (7-13) highlights the advantage of increasing the cross-coupling capacitance C_3 rather than C_1, because C_3 is amplified by a factor of about 2 (C_1 being approximately equal to C_2).

5. Comparison with experimental data

To determine the SEU threshold of a memory cell, the final step consists in comparing at each time Q_{crit}, provided by the analytical model independently of the ion hit, and Q_{col}, obtained by means of a restricted number of numerical simulations. Three-dimensional Davinci simulations [27] are required to avoid some artifacts of 2D-simulations. The cell upsets at the smallest time t such that $Q_{col}(t) > Q_{crit}(t)$. Figure 7.15 shows $Q_{crit}(t)$, with V_{dd} as parameter, and $Q_{col}(t)$, with the tilt angle as parameter. $Q_{col}(t)$ is only computed for V_{dd} = 1.9V. This is sufficient since Q_{col} is not strongly sensitive to V_{dd}.

Although the parameters used for Davinci simulations are not optimized to represent experimental devices, it emerges that the supply voltage must be lowered between 2V and 1.5V, and the tilt angle increased above 70°, in order to produce a cell upset. Furthermore, at V_{dd} = 3V, the cell is clearly insensitive even to horizontal strikes (θ = 90°). At V_{dd} = 1.5V, the cell is upset-immune for θ < 40°. This clearly matches experimental results shown in Figures 7.1 and 7.2 where the maximum cross-section is not reached but the sensitivity exponentially rises when V_{dd} is lowered below 2V with θ = 70°. It clearly appears that the comparison of the asymptotic values $Q_{crit}(0)$ and $Q_{col}(\infty)$, as usually performed, is not sufficient to determine the cell sensitivity. The introduction of the temporal dimension is mandatory. Moreover, Figure 7.15 shows that the critical

time at which the cell upsets is a complex function of three parameters: C_T, V_{dd}, and $Q_{inj}(\theta)$. Therefore, it is not obvious to define *a priori* an adequate time at which Q_{crit} and Q_{col} must be compared. Finally, the graphical method is very convenient to quickly obtain a rough idea of the upset conditions owing to the separation of the parameters influencing the collected charge on one hand and the critical charge on the other hand.

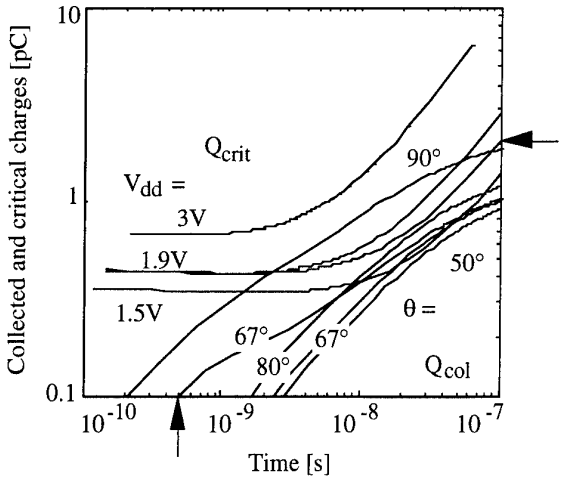

Figure 7.15: Collected and critical charges as a function of time with the tilt angle and the supply voltage as parameter, respectively. Q_{col} is obtained by 3D-Davinci simulations and V_{dd} = 1.9V. Q_{crit} is provided by the analytic model.

Two reasons can be pushed beyond to explain the measurement spreading observed around the SEU threshold in Figure 7.1.

• The influence of total dose

Total-dose is susceptible to reduce the carrier lifetime τ (displacement damages). Figure 7.11 shows that a variation of τ only induces a modification of the amplification gain for $t > 10^{-7}$s, while Figure 7.15 indicates that the cell upset occurs around 10^{-8}s. Therefore, the collected charge should be unaffected by displacement damages up to the upset point. Another effect of total-dose is to reduce the p-type gate voltage overdrive V_{dd}-V_G+V_{thp} (since the p-channel threshold decreases with irradiation). The critical charge for cell upset is subsequently changed through a reduction of $I_{P1,sat}$. The breaking point moves to the right so that the cell is upset sensitive for a longer time (as indicated by the Q_{crit}-curve pointed by the horizontal arrow in Figure 7.15 for V_{dd} = 1.9V). As a consequence, the soft-error sensitivity of n-hits should increase with dose which is in contradiction with the results exposed in Reference [28] on the basis of a purely static approach.

• The influence of statistical fluctuations

The statistical distribution of hit locations is usually mentioned to generate both measurement spreading and gradual increase of the cross-section [29]. In SOI devices, the SEU sensitivity to the position of the strike is usually explained by the variation of the bipolar amplification gain as a function of the distance between the ion impact and the body tie. The GAA structure could be sensitive to the ion strike location as well, but the reason is different since there is no body contact: the funneling-like charge collection occurs earlier for hits located closer to the drain junction (Q_{col}-curve pointed by the

vertical arrow for $\theta = 67°$ in Figure 7.15). Nevertheless, Figure 7.15 shows that the hit position could only affect the switching at very low supply voltages.

Also, the very small number (1...20) of cell upsets recorded around the SEU threshold enhances the statistical spreading effect. Finally, it should be mentioned that we have not examined if a single cell was upset more than once during the exposure or if a single particle induced upsets in more than one cell (simultaneous upsets).

6. Conclusions

A 1k GAA SRAM has been exposed to a beam of heavy particles. An exceptional SEU hardness has been highlighted: normal cross-sections less than 3×10^{-8}[cm^2/bit] are obtained for LET_{eff} up to 170[MeV.cm^2/mg] at a supply voltage as low as 1.9V. An explanation split in three points was proposed. The limitation of the injected charge by thin Si films (thinner than the radial distribution of the track), when grazing ion beams are involved, is partially responsible for the results. Secondly, simulations showed that the charge collection mechanisms are very slow in GAA devices and that bipolar amplification is delayed. The large source/drain series resistances, due to the particular geometry of the device, the low supply voltage, and high injection conditions are responsible for this delay. Finally, it was shown that the critical charge may no longer be assumed to be constant during the slow collection phase. A new method for the determination of the cell upset condition was then proposed which consists in including time as a new variable. An analytical general model describing the temporal dependence of the critical charge as a function of supply voltage and capacitances was derived independently of the pulse shape generated by the ion. In the light of this model, it becomes clear that the naturally high Miller capacitances of the GAA memory cell allows to reduce the supply voltage for the same initial SEU hardness. However, at reduced supply voltage, the cell is upset sensitive during a longer time. Finally, the net competition between slow charge collection and longer upset sensitivity was shown to be favorable to the SEU hardness for supply voltages lowered down to 2V, as experimentally observed.

The above analysis was performed for the limit of transient response for one particle. Since gamma-dot experiments (high-dose rate flash irradiations) have not been performed, we are not able to discuss true transient events generated from a weapon. However, we expect the GAA structure to successfully operate at reduced temperature in a high dose rate environment for the readout electronics as well.

Annex I

The CYCLONE accelerator of Louvain-la-Neuve, Belgium, is a variable energy multiparticle facility capable to accelerate protons up to 90[MeV] and heavy ions up to $110Q^2/M$[MeV] with Q the ion charge and M its atomic mass. Heavy ions are produced by an external Electron Cyclotron Resonant (ECR) source, extracted from the source, analyzed and finally injected in the cyclotron. The beams are composed of different ions with very close mass over charge ratios. Two different cocktails are available. The energy E, Linear Energy Transfer LET and range in silicon of the beam adopted for the experiments are listed in Table A1. The selection of a precise ion is made by a fine adjustment of the magnetic field or the HF frequency of the cyclotron.

Table A1: Characteristics of the ion beam used for the SEU test of the 1k GAA SRAM. M/Q = 5, E = 4.4MeV/AMU.

Ion	Energy [MeV]	LET [MeVcm^2/mg]	Range in Si [µm]
$^{40}Ar^{5+}$	150	14.1	42
$^{20}Ne^{4+}$	78	5.85	45
$^{15}N^{3+}$	62	2.97	64
$^{132}Xe^{26+}$	459	55.9	43
$^{84}Kr^{17+}$	316	34	43

A Parallel Plate Avalanche Counter (PPAC) gives the number of particles that reach the Device Under Test (DUT) during SEU measurements. The calibration of the PPAC has been performed by temporarily inserting in the beam a Passivated Implanted Planar Silicon (PIPS) detector which has exactly a section of one square centimeter. Let r be the ratio between the independent counts of the PPAC and the PIPS detectors during the calibration procedure (r = #PPAC/#PIPS). The total number of particles flowing through one square centimeter of the DUT during exposure is then given by #PPAC/r [cm^{-2}]. The total cross-section of the memory is obtained in square centimeter unit as:

$$\sigma\left[cm^2\right] = \frac{\#SEU \cdot r}{\#PPAC}$$

with #SEU, the number of upsets recorded in the DUT, and #PPAC, the particle count given by the PPAC. The vertical and horizontal homogeneity as well as the purity of the beam have been verified.

During SEU measurements, SRAMs are controlled by an HP16500B Logic Analysis System (itself supervised by a PC through GPIB connections). Memories are filled with a checkerboard pattern and then placed in the "on-line" or "isolated" mode. In the "on-line" mode, the DUT is continuously read during irradiation so that, if a SEU is observed, the error could be immediately corrected and the event recorded. In the "isolated" mode, the memory is disconnected from the Logic Analysis System and irradiated. When the

irradiation is stopped, the memory is read and the number of errors is recorded. Preliminary measurements were performed on the commercially available 2k×8 SRAM HM-65162 from Matra Harris in "on-line" mode to check the validity of the experimental set-up. The total cross-section obtained for one of the two available kbits of the memory with an Ar beam (Table A1) under a supply voltage of 5V is:

$$\sigma = \frac{\#SEU \cdot r}{\#PPAC} = \frac{6 \cdot 3.8}{5770} = 3.95 \times 10^{-3} [cm^2]$$

This measurement agrees well with the total cross-section obtained by the ESA/ESTEC at the GSI Darmstadt [30] and therefore give us confidence for the rest of the experiment.

Annex II

The different fixed parasitic capacitances of the GAA device are depicted in Figure 7.6. Recalling that the minimum drawing feature sizes are L = W = 3μm, and that the effective sizes are W_{eff} = 2.2μm and L_{eff} = 2.4μm (L-L_{eff} = 2ΔL = 0.6μm), we obtain, for a square minimum-size transistor:

- the overlap capacitances:
  $C_{gso} = C_{gdo} = C_{oxf} \cdot (L/2+2\Delta L) \cdot W_{eff} = 5.32[fF]$
- the source/drain-to-substrate capacitances:
  $C_{dbo} = C_{sbo} = C_{oxb}C_{si,sub}/(C_{oxb}+C_{si,sub}) \cdot \gamma = 1.49[fF]$
  ($\gamma = 31.44$ [μm²] is a geometrical factor extracted from the layout)
- the back-gate-to-substrate capacitances:
  $C_{gbo} = C_{oxf}C_{si,sub}/(C_{oxf}+C_{si,sub}) \cdot (L+L/2+L/2) \cdot W_{eff} = 1.26[fF]$

with :

- for the gate oxide: $C_{oxf} = \varepsilon_{ox}/t_{oxf} = 1.151[fF/\mu m^2]$, $t_{oxf} = 30nm$
- for the buried oxide: $C_{oxb} = \varepsilon_{ox}/t_{oxb} = 0.088[fF/\mu m^2]$, $t_{oxb} = 390nm$
- in the substrate: $C_{si,sub} = \varepsilon_{si}/x_{dmax,sub} = 0.103[fF/\mu m^2]$,
  $x_{dmax,sub} = 1.025\mu m$ assuming $N_{A,sub} = 7\times e^{14}[cm^{-3}]$

For each transistor of the memory cell, the gate-to-source/drain capacitances are determined from the transistor regime at the beginning of the ion strike [20] (Figure 7.7): $C_{gs} = C_{gd} = 0.5C_{ox}$ for a transistor in linear regime, $C_{gs} = 2C_{ox}/3$, $C_{gd} = 0$ for a saturated device with $C_{ox} = 2W_{eff} L_{eff} C_{oxf} = 12[fF]$. Since $M_N = 4$, $M_P = 1$ and $M_A = 1$ are the number of minimum size square devices placed in parallel to form the driver, load and access devices of the memory cell respectively, the total capacitances C_1, C_2 and C_3 of the memory cell, as shown in Figure 7.7, are:

$$C_1 = (M_P+M_N+M_A)(C_{gdo}+C_{dbo}) + (M_P+M_N) C_{gbo} + (2/3\ M_P + 1/2\ M_N) C_{ox}$$

$$C_2 = (M_P+M_N+M_A)(C_{gdo}+C_{dbo}) + (M_P+M_N) C_{gbo} + (1/2\ M_P + 2/3\ M_N) C_{ox}$$

$$C_3 = 2 (M_P+M_N) C_{gdo} + (1/2\ M_P + 1/2\ M_N) C_{ox}$$

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Conclusion

We have treated various aspects concerning a new MOSFET derived from the Silicon-On-Insulator (SOI) process. The new surrounding gate device consists of a thin silicon channel region totally wrapped in a thin high-quality gate oxide which is itself totally surrounded by a polysilicon gate. The transistor therefore operates like two symmetrical MOS transistors, one at the front and the other at the back interface of the active silicon region, sharing the same thin silicon volume. When the silicon film thickness is sufficiently reduced in order to achieve full depletion, the so-called Gate-All-Around (GAA) device should provide the ultimate (or ideal) MOS performance. Indeed, the substrate influence is totally shielded by the back portion of the gate, the body conduction is favored, and both front and back interfaces contribute equally to the current flow. Compared to regular SOI transistors, the GAA device should also benefit from the absence of the buried oxide below the channel as far as self-heating and total-dose irradiation hardness are concerned. We demonstrated experimentally and theoretically that the near-optimum behavior really exists and is preserved for operation in harsh environments such as high temperature and irradiation exposure.

Chapter I described the fabrication process.

Being fully compatible with the regular self-aligned SOI process, the GAA fabrication is very simple and requires only one additional masking step and wet etch step to locally groove a cavity in the buried oxide. The active silicon bar, hanging like a bridge, is then surrounded by the gate oxide and the polysilicon gate. Layout and scaling rules were discussed. When the cavity etching is not optimized, parasitic resistances/capacitances are quite large. Also, the layout is not compact and the device could not be scaled below the micron-range. However, measurements confirm the expected electrical advantages of the GAA structure over the SOI counterpart, such as higher current and transconductance, steeper subthreshold slope and smaller output conductance.

Chapter II dealt with device modeling.

The numerous electrical advantages of the double-gate MOS transistor lie on the concept of volume inversion yielded by the optimum gate-to-body coupling: the carriers are no longer confined near the surface, but are found across the whole film. Since the resulting potential distribution is unique and quite different from that in bulk and single-gate SOI MOSFETs, classical analyses fail. Taking simultaneously into account both the dopant impurity charges and the minority carrier concentration, we obtained, for n-channel devices in linear operation, one-dimensional models continuously valid and accurate from subthreshold to strong inversion regimes. They significantly outperform previous studies in terms of physical insight on the volume inversion mechanisms and

range of validity. A first approach provides the distribution of the potential across the film, from which expressions of the current and the transconductance are derived. This model is accurate even if process parameters are varied by orders of magnitude. Another approach provides a very robust expression of the threshold voltage. This study also enabled us to clarify the debate about the improvement of the current and the transconductance by more than a factor two over conventional SOI devices: a significant enhancement should only be observed owing to higher volume mobility, below and around threshold, especially in lightly doped films. Finally, we gave an explicit expression of the subthreshold current, more accurate than the usual formulation. The subthreshold slope is nearly ideal, confirming the perfect control of the channel potential by the surrounding gate.

Chapter III focused on operation at elevated temperatures.

Bulk MOSFETs usually cease to function in the range 200...250°C due to excessive junction leakage currents and threshold voltage drifts. SOI circuits offer a nice alternative owing to their perfect isolation and small drain junction areas that drastically reduce leakage. Fully-depleted SOI transistors furthermore provide minimum threshold voltage roll-off with temperature. We first proved (theoretically and experimentally) that, in GAA structures, the minimum threshold voltage sensitivity is maintained up to a higher temperature than in SOI devices. In addition, we showed that the ratio between the on-state current and the leakage diffusion current is at least a factor of 2 larger in GAA devices than in their SOI counterparts, up to 300°C. Measurements on simple digital circuits then confirmed that the GAA technology has a strong potential to successfully realize both static and dynamic logic circuits that must operate at high temperature. This can be helpful for various applications such as automotive, well logging, aircraft, spacecraft as well as in the nuclear industry.

Chapter IV was dedicated to the self-heating analysis important for power applications.

One of the drawback of the thick buried oxide in SOI is its poor thermal conductivity. Self-heating effects appear when a large power is dissipated: the carrier mobility is reduced as a result of the channel temperature elevation, and causes a negative differential conductance in saturation operation. Thinning down the buried oxide layer has been proposed to enhance the heat flow towards the substrate but results in loss of the SOI speed advantage due to the increase of parasitic capacitances with the substrate. We highlighted that the use of GAA devices is favorable to reduce self-heating problems. From the heating viewpoint, the GAA channel region is indeed only separated from the substrate by two thin layers of gate oxide which substantially enhances the heat evacuation. On the other hand, source and drain regions still lie on the thick buried oxide layer and their parasitic capacitances with the substrate are kept small (nevertheless, the gate-to-substrate and overlap capacitances are increased). Starting from a well-known model, a general detailed discussion of the heat transfer is performed for SOI devices as a function of the buried oxide thickness. The heat evacuation is shown to follow $(t_{oxb})^{-n}$ with $0.5 < n < 1$ and strongly depends on device dimensions. The specific equivalent global thermal conductance of the GAA structure was computed as well. In a second step, three independent experimental evidences of enhanced heat evacuation in GAA transistors were provided and analyzed. Each time, the analytically predicted thermal conductance

qualitatively explains experimental data though the model suffers from the uniform temperature approximation.

In the last three chapters, V to VII, we focused on the tremendous benefits brought by the GAA process for numerous applications requiring a high level of radiation-hardening. The bulk technology is known to sustain quite large levels of cumulated dose of irradiation but is very sensitive to transient events due to a funneling effect which collects charges generated deeply into the substrate. The SOI technology solves this problems owing to the complete isolation of the channel from the substrate. Nevertheless, the total-dose hardness of SOI fully-depleted devices is often strongly degraded by the presence of the thick buried oxide layer. Permanent radiation damages are indeed dependent on the thickness of the oxide layers in contact with the channel. Charge trapping is minimized in GAA devices because the channel is only surrounded by a thin layer of high quality gate oxide. On the other hand, like in SOI transistors, the perfect isolation of the thin active region efficiently limits the charges collected during a heavy particle strike. As a consequence, the GAA structure provides the best hardening-by-technology approach and combines both the hardness of bulk, against total-dose irradiation effects, and of SOI, against transient events. This combination makes GAA devices particularly suitable for space, military or nuclear industry applications.

In Chapter V, measurements performed on discrete GAA devices up to 85Mrad(Si) total-dose irradiation showed that the variation of electrical parameters should allow circuit operation up to the highest dose. This is a good news, especially if we keep in mind that the process is not specially optimized for radiation hardness. We also pointed out that the GAA geometry provides the interesting property that no edge leakage current could appear upon irradiation exposure. GAA transistors are therefore promising candidates for digital as well as analog applications in high total-dose environments and meets the requirements of the most advanced nuclear projects.

The efficiency of methods using circuit design skills to improve total-dose performance of SOI CMOS SRAMs was discussed in Chapter VI. The main problems of the soft SOI process are large negative threshold voltage shifts and leakage currents in n-channel devices, created by charge trapping in the buried oxide. First, several modified designs were proposed to stabilize the transfer characteristic of CMOS inverters. The "pull-up" configuration helps to keep a full logic swing, while the "diode-pair" configuration minimizes the shift of the inverter's switching point. Buffers including both "pull-up" and "diode-pair" stages combine both these advantages. This local compensation approach can be extended to all peripheral circuits of an SRAM including differential read amplifiers. The drawback of the method is to consume a large silicon real estate especially if no speed reduction is allowed. For this reason, compensation circuits cannot be added to the cross-coupled inverters of SRAM cells which are therefore the weakest elements of static memories. The stability of the classical six-transistor memory cell was discussed as a function of dose in retention mode and during read and write operations. It was shown that memory failure linked to leakage currents in n-channel devices cannot be overcome by proper design, except by using p-type accessed cells. The tremendous drawback of this solution is the drastic increase of the memory access time.

The only practical solution hence consists in limiting the threshold voltage shifts to reasonable values. The GAA technology being the perfect candidate, its potentiality has been demonstrated with a 1k SRAM still functional after 85Mrad(Si) irradiation.

Finally, Chapter VII investigated the Single-Event-Upset (SEU) sensitivity of 1k GAA SRAMs. Surprisingly, experimental results obtained with a supply voltage of 2V are much better than those published for equivalent SOI circuits operated at a higher supply voltage. The limitation of the injected charge by the thin Si film (thinner than the radial distribution of the track), when grazing ion beams are involved, is partially responsible for the results. The second piece of explanation is that collection mechanisms and bipolar amplification are delayed in GAA devices. The large source/drain series resistances, due to the particular geometry of the device, the low supply voltage and high injection conditions are responsible for this delay. The last important point is that partial recovery of the initial state of the memory cell occurs during the slow collection process, in such a manner that the critical charge for upset increases. The determination of the cell upset conditions based on a purely static approach is therefore no longer valid. To solve this problem, we proposed a general analytical model describing the time-dependence of the critical charge, independently of the current pulse shape generated by the ion hit. In the light of this model, it becomes clear that the naturally high Miller capacitances of the GAA memory cell allows to reduce the supply voltage for the same initial SEU hardness. However, at reduced supply voltage, the cell is upset sensitive during a longer time. Finally, the net competition between slow charge collection and longer upset sensitivity is shown to be favorable to the SEU hardness for supply voltages lowered down to 2V, as experimentally observed.

We have mainly focused our attention on digital circuits. The radiation-hard analog conception in general is indeed at its very beginning but interests an increasing number of teams. Transconductance and output conductance measurements performed in normal, high temperature and radiation environments, indicate that GAA devices should be highly profitable to analog designs as well. However, neither the high temperature nor the total-dose behavior of the output conductance, crucial parameter for analog design, is correctly understood at the present time. The way is left open for future very interesting investigations.

List of Publications

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